



AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B																																							
26:21	Reserved	Project: All	Format:																																				
20:16	Convertor_Channel_Count See Conv A description.	Project: All	Format:																																				
15	Reserved	Project: All	Format:																																				
14	Sample_Base_Rate Project: All Default Value: 0b 48 kHz See Conv A description.																																						
	<table border="1"> <thead> <tr> <th>Value Na</th> <th>me</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>48 kHz</td> <td>48 kHz</td> <td>All</td> </tr> <tr> <td>1b</td> <td>44.1 kHz</td> <td>44.1 kHz</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	0b	48 kHz	48 kHz	All	1b	44.1 kHz	44.1 kHz	All																										
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13:11	Sample_Base_Rate_Mult Project: All Default Value: 000b 48 kHz See Conv A description.																																						
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10:8	Sample_Base_Rate_Divisor Project: All Default Value: 000b 48 kHz See Conv A description.																																						
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AUD_OUT_STR_DESC_B—Audio Stream Descriptor Format – Conv B																													
7	Reserved Project: All Format: MBZ																												
6:4	<p>Bits_per_Sample Project: All Default Value: 011b 32 bits</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>8 bit</td> <td>The data will be packed in memory in 8 bit containers on 16 bit boundaries</td> <td>All</td> </tr> <tr> <td>001b</td> <td>16 bits</td> <td>The data will be packed in memory in 16 bit containers on 16 bit boundaries</td> <td>All</td> </tr> <tr> <td>100b</td> <td>20 bits</td> <td>The data will be packed in memory in 20 bit containers on 32 bit boundaries</td> <td>All</td> </tr> <tr> <td>010b</td> <td>24 bits</td> <td>The data will be packed in memory in 24 bit containers on 32 bit boundaries</td> <td>All</td> </tr> <tr> <td>011b</td> <td>32 bits</td> <td>The data will be packed in memory in 32 bit containers on 32 bit boundaries</td> <td>All</td> </tr> <tr> <td>others</td> <td>Res.</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	000b	8 bit	The data will be packed in memory in 8 bit containers on 16 bit boundaries	All	001b	16 bits	The data will be packed in memory in 16 bit containers on 16 bit boundaries	All	100b	20 bits	The data will be packed in memory in 20 bit containers on 32 bit boundaries	All	010b	24 bits	The data will be packed in memory in 24 bit containers on 32 bit boundaries	All	011b	32 bits	The data will be packed in memory in 32 bit containers on 32 bit boundaries	All	others	Res.	Reserved	All
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011b	32 bits	The data will be packed in memory in 32 bit containers on 32 bit boundaries	All																										
others	Res.	Reserved	All																										
3:0	<p>Number_of_Channels_in_a_Stream Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111 = 16 See Conv A description.</p>																												

4.2.14.1 AUD_PINW_CONNLNG_LIST—Audio Connection List

AUD_PINW_CONNLNG_LIST—Audio Connection List	
<p>Register Type: MMIO Address Offset: E20A8h Project: All Default Value: 00000302h Access: Read Only Size (in bits): 32</p>	
These values are returned from the device as the Connection List Length response to a Get Pin Widget command.	
Bit De	scription
31:16	Reserved Project: All Format:



AUD_PINW_CONNLNG_LIST—Audio Connection List	
15:8	Connection_List_Entry Project: All Default Value: 03h Connection to Convertor Widget Node 0x03
7	Long_Form Project: All Default Value: 0b This bit indicates whether the items in the connection list are 'long form' or 'short form'. This bit is hardwired to 0 (items in connection list are short form)
6:0	Connection_List_Length Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

4.2.15 AUD_PINW_CONNLNG_SEL—Audio Connection Select

AUD_PINW_CONNLNG_SEL—Audio Connection Select	
Register Type: MMIO Address Offset: E20ACh Project: All Default Value: 00000000h Access: Read Only Size (in bits): 32	
These values are returned from the device as the Connection List Length response to a Get Pin Widget command.	
Bit De	scription
31:24	Reserved Project: All Format:
23:16	Connection_select_Control_D Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	Connection_select_Control_C Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	Connection_select_Control_B Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00



4.2.16 AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

AUD_CNTL_ST_A—Audio Control State Register – Transcoder A			
Register Type: MMIO Address Offset: E20B4h Project: All Default Value: 00005400h Access: R/W Size (in bits): 32			
Bit De	scription		
31	Reserved	Project: All	Format: MBZ
30:29	DIP_Port_Select Project: All Access: Read Only Default Value: 00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed.		
	Value Name	Description	Project
	00b	Reserved	All
	01b	Digital Port B	All
	10b	Digital Port C	All
	11b	Digital Port D	All
28:25	Reserved	Project: All	Format: MBZ



AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

24:21	<p>DIP_type_enable_status</p> <p>Project: All</p> <p>Access: Read Only</p> <p>Default Value: 0000b</p> <p>These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 10%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>XXX0b</td> <td>Disable</td> <td>Audio DIP disabled</td> <td>All</td> </tr> <tr> <td>XXX1b</td> <td>Enable</td> <td>Audio DIP enabled</td> <td>All</td> </tr> <tr> <td>XX0Xb</td> <td>Disable</td> <td>Generic 1 (ACP) DIP disabled</td> <td>All</td> </tr> <tr> <td>XX1Xb</td> <td>Enable</td> <td>Generic 1 (ACP) DIP enabled</td> <td>All</td> </tr> <tr> <td>X0XXb</td> <td>Disable</td> <td>Generic 2 DIP disabled</td> <td>All</td> </tr> <tr> <td>X1XXb</td> <td>Enable</td> <td>Generic 2 DIP enabled, can be used by ISRC1 or ISRC2</td> <td>All</td> </tr> <tr> <td>1XXXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	XXX0b	Disable	Audio DIP disabled	All	XXX1b	Enable	Audio DIP enabled	All	XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All	XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All	X0XXb	Disable	Generic 2 DIP disabled	All	X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All	1XXXb	Reserved	Reserved	All
Value Na	me	Description	Project																														
XXX0b	Disable	Audio DIP disabled	All																														
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1XXXb	Reserved	Reserved	All																														
20:18	<p>DIP_buffer_index</p> <p>Project: All</p> <p>Default Value: 0000b</p> <p>This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 10%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 20%;">Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Audio</td> <td>Audio DIP (31 bytes of address space, 31 bytes of data)</td> <td>All</td> </tr> <tr> <td>001b</td> <td>Gen 1</td> <td>Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> <td>All</td> </tr> <tr> <td>010b</td> <td>Gen 2</td> <td>Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> <td>All</td> </tr> <tr> <td>011b</td> <td>Gen 3</td> <td>Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All	001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)	All	010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All	011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All	1XXb	Reserved	Reserved	All								
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1XXb	Reserved	Reserved	All																														



AUD_CNTL_ST_A—Audio Control State Register – Transcoder A

17:16	DIP_transmission_frequency	Project: All	Access: Read Only	Default Value: 00b	<p>These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.</p> <p>When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 10%;">Value Na</th> <th style="width: 10%;">me</th> <th style="width: 50%;">Description</th> <th style="width: 10%;">Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> <td>Disabled</td> <td>All</td> </tr> <tr> <td>01b</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> <tr> <td>10b</td> <td>Send Once</td> <td>Send Once</td> <td>All</td> </tr> <tr> <td>11b</td> <td>Best Effort</td> <td>Best effort (Send at least every other vsync)</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	00b	Disable	Disabled	All	01b	Reserved	Reserved	All	10b	Send Once	Send Once	All	11b	Best Effort	Best effort (Send at least every other vsync)	All
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00b	Disable	Disabled	All																						
01b	Reserved	Reserved	All																						
10b	Send Once	Send Once	All																						
11b	Best Effort	Best effort (Send at least every other vsync)	All																						
15	Reserved	Project: All	Format: MBZ																						
14:10	ELD_buffer_size	Project: All	Access: Read Only		10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)																				
9:5	ELD_access_address	Project: All			Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.																				
4	ELD_ACK	Project: All			Acknowledgement from the audio driver that ELD read has been completed																				
3:0	DIP_RAM_access_address	Project: All			Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.																				



4.2.17 AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

AUD_CNTL_ST_B—Audio Control State Register – Transcoder B			
Register Type: MMIO Address Offset: E21B4h Project: All Default Value: 00005400h Access: R/W Size (in bits): 32			
Bit De	scription		
31	Reserved	Project: All	Format: MBZ
30:29	DIP_Port_Select Project: All Access: Read Only Default Value: 00b See Transcoder A description.		
	Value Na	me	Description
	00b	Reserved	Reserved
	01b	Digital Port B	Digital Port B
	10b	Digital Port C	Digital Port C
	11b	Digital Port D	Digital Port D
28:25	Reserved	Project: All	Format: MBZ
24:21	DIP_type_enable_status Project: All Access: Read Only Default Value: 0000b See Transcoder A description.		
	Value Na	me	Description
	XXX0b	Disable	Audio DIP disabled (Default)
	XXX1b	Enable	Audio DIP enabled
	XX0Xb	Disable	Generic 1 (ACP) DIP disabled
	XX1Xb	Enable	Generic 1 (ACP) DIP enabled
	X0XXb	Disable	Generic 2 DIP disabled
	X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2
	1XXXb	Reserved	Reserved



AUD_CNTL_ST_B—Audio Control State Register – Transcoder B

20:18	<p>DIP_buffer_index Project: All Default Value: 000b See Transcoder A description.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value Na</th> <th style="text-align: center;">me</th> <th style="text-align: left;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td style="text-align: center;">Audio</td> <td>Audio DIP (31 bytes of address space, 31 bytes of data)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">001b</td> <td style="text-align: center;">Gen 1</td> <td>Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">010b</td> <td style="text-align: center;">Gen 2</td> <td>Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">011b</td> <td style="text-align: center;">Gen 3</td> <td>Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1XXb</td> <td style="text-align: center;">Reserved</td> <td>Reserved</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All	001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data)	All	010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All	011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All	1XXb	Reserved	Reserved	All
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1XXb	Reserved	Reserved	All																						
17:16	<p>DIP_transmission_frequency Project: All Access: Read Only Default Value: 00b See Transcoder A description</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value Na</th> <th style="text-align: center;">me</th> <th style="text-align: left;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">Disable</td> <td>Disabled</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">01b</td> <td style="text-align: center;">Reserved</td> <td>Reserved</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">Send Once</td> <td>Send Once</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">Best Effort</td> <td>Best effort (Send at least every other vsync)</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	00b	Disable	Disabled	All	01b	Reserved	Reserved	All	10b	Send Once	Send Once	All	11b	Best Effort	Best effort (Send at least every other vsync)	All				
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00b	Disable	Disabled	All																						
01b	Reserved	Reserved	All																						
10b	Send Once	Send Once	All																						
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9:5	<p>ELD_access_address Project: All See Transcoder A description.</p>																								
4	<p>ELD_ACK Project: All See Transcoder A description.</p>																								
3:0	<p>DIP_RAM_access_address Project: All See Transcoder A description.</p>																								



4.2.18 AUD_CNTL_ST2— Audio Control State 2

AUD_CNTL_ST2— Audio Control State 2			
Register Type: MMIO Address Offset: E20C0h Project: All Default Value: 00000000h Access: R/W Size (in bits): 32			
This register is used for handshaking between the audio and video drivers for interrupt management. For each port, ELD readiness is sent by the display software to the audio software via an unsolicited response when the ELD or CP ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital display port.			
Bit De	scription		
31:10	Reserved	Project: All	Format:
9	CP_ReadyD Project: All Default Value: 0b This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced.		
	Value Name	Description	Project
	0b	Pending or Not Ready	All
	1b	Ready	All
8	ELD_validD Project: All Default Value: 0b This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.		
	Value Name	Description	Project
	0b	Invalid	All
	1b	Valid	All
7:6	Reserved	Project: All	Format:



AUD_CNTL_ST2— Audio Control State 2

5	<p>CP_ReadyC Project: All Default Value: 0b See CP_ReadyD description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Ready</td> <td>CP request pending or not ready to receive requests</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Ready</td> <td>CP request ready</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Not Ready	CP request pending or not ready to receive requests	All	1b	Ready	CP request ready	All
Value	Name	Description	Project										
0b	Not Ready	CP request pending or not ready to receive requests	All										
1b	Ready	CP request ready	All										
4	<p>ELD_validC Project: All Default Value: 0b See ELD_validD description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Invalid</td> <td>ELD data invalid (default, when writing ELD data, set 0 by software)</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Valid</td> <td>ELD data valid (Set by video software only)</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All	1b	Valid	ELD data valid (Set by video software only)	All
Value	Name	Description	Project										
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All										
1b	Valid	ELD data valid (Set by video software only)	All										
3:2	<p>Reserved Project: All Format:</p>												
1	<p>CP_ReadyB Project: All Default Value: 0b See CP_ReadyD description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Ready</td> <td>CP request pending or not ready to receive requests</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Ready</td> <td>CP request ready</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Not Ready	CP request pending or not ready to receive requests	All	1b	Ready	CP request ready	All
Value	Name	Description	Project										
0b	Not Ready	CP request pending or not ready to receive requests	All										
1b	Ready	CP request ready	All										
0	<p>ELD_validB Project: All Default Value: 0b See ELD_validD description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Invalid</td> <td>ELD data invalid (default, when writing ELD data, set 0 by software)</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Valid</td> <td>ELD data valid (Set by video software only)</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All	1b	Valid	ELD data valid (Set by video software only)	All
Value	Name	Description	Project										
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All										
1b	Valid	ELD data valid (Set by video software only)	All										



4.2.19 AUD_HDMIW_STATUS—Audio HDMI Status

AUD_HDMIW_STATUS—Audio HDMI Status	
Register Type: MMIO Address Offset: E20D4h Project: All Security: Debug Default Value: 00000000h Access: R/W Clear Size (in bits): 32	
Bit De	scription
31	Conv_B_CDCLK/DOTCLK_FIFO_Underrun Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
30	Conv_B_CDCLK/DOTCLK_FIFO_Ovrrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
29	Conv_A_CDCLK/DOTCLK_FIFO_Underrun Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
28	Conv_A_CDCLK/DOTCLK_FIFO_Ovrrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
27:26	Reserved Project: All Format:
25	BCLK/CDCLK_FIFO_Ovrrun Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
24	Function_Reset Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
23:0	Reserved Project: All Format:



4.2.20 AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A

AUD_HDMIW_HDMIEDID_A—HDMI Data EDID Block – Transcoder A	
Register Type: MMIO Address Offset: E2050h Project: All Default Value: 00000000h Access: R/W Size (in bits): 32	
<p>These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command.</p> <p>Writing sequence:</p> <ul style="list-style-type: none"> - Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written. - Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. - Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. <p>Reading sequence:</p> <ul style="list-style-type: none"> - Video software sets the ELD access address to 0, or to the desired DWORD to be read. - Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached. 	
Bit De	scription
31:0	EDID_HDMI_Data_Block Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset



4.2.21 AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Transcoder B

AUD_HDMIW_HDMIEDID_B—HDMI Data EDID Block – Transcoder B	
Register Type: MMIO	
Address Offset: E2150h	
Project: All	
Default Value: 00000000h	
Access: R/W	
Size (in bits): 32	
See Transcoder A description.	
Bit De	scription
31:0	EDID_HDMI_Data_Block See Transcoder A description
	Project: All Format:



4.2.22 AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A

AUD_HDMIW_INFOFR_A—Audio Widget Data Island Packet – Transcoder A	
Register Type:	MMIO
Address Offset:	E2054h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32
<p>When the IF type or dword index is not valid, the contents of the DIP will return all 0's. These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI DIP get. Video driver read sequence (for debug only): Video software sets DIP type to the appropriate DIP, and sets the DIP access address to the desired DWORD. Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached.</p>	
Bit De	scription
31:0	<p>Data_Island_Packet_Data Project: All Format:</p> <p>This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.</p>

4.2.23 AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Transcoder B

AUD_HDMIW_INFOFR_B—Audio Widget Data Island Packet – Transcoder B	
Register Type:	MMIO
Address Offset:	E2154h
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32
See Transcoder A description.	
Bit De	scription
31:0	<p>Data_Island_Packet_Data Project: All Format:</p> <p>See Transcoder A description.</p>



4.3 DPB Control and Aux Channel

4.3.1 DPB—DisplayPort B Control Register

DPB—DisplayPort B Control Register															
Register Type:	MMIO														
Address Offset:	E4100h														
Project:	All														
Default Value:	00000018h														
Access:	R/W														
Size (in bits):	32														
Double Buffer Update Point:	Depends on bit														
Please note that DisplayPort B uses the same lanes as HDMIB. Therefore +B/HDMIB and DisplayPort B cannot be enabled simultaneously.															
Bit De	scription														
31	<p>DisplayPort_B_Enable</p> <p>Project: All</p> <p>Default Value: 0b</p> <p>Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written.</p> <p>[DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMIB from being enabled on transcoder A.</p> <table border="1"> <thead> <tr> <th>Value Na</th> <th>me</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Disable and tristates the Display Port B interface</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enable. This bit enables the Display Port B interface</td> <td>All</td> </tr> </tbody> </table>			Value Na	me	Description	Project	0b	Disable	Disable and tristates the Display Port B interface	All	1b	Enable	Enable. This bit enables the Display Port B interface	All
Value Na	me	Description	Project												
0b	Disable	Disable and tristates the Display Port B interface	All												
1b	Enable	Enable. This bit enables the Display Port B interface	All												



DPB—DisplayPort B Control Register

30	Transcoder_Select	Project: All Default Value: 0b	This bit determines from which display transcoder the source data will originate. Transcoder selection takes place on the Vblank after being written [DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.																				
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Transcoder A</td> <td>Transcoder A</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Transcoder B</td> <td>Transcoder B</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Transcoder A	Transcoder A	All	1b	Transcoder B	Transcoder B	All								
Value	Name	Description	Project																				
0b	Transcoder A	Transcoder A	All																				
1b	Transcoder B	Transcoder B	All																				
29:28	Link_training_pattern_enable	Project: All Default Value: 0b	These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.																				
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 60%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Pattern 1</td> <td>Pattern 1 enabled: Repetition of D10.2 characters</td> <td>All</td> </tr> <tr> <td>01b</td> <td>Pattern 2</td> <td>Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.</td> <td>All</td> </tr> <tr> <td>10b</td> <td>Idle</td> <td>Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times</td> <td>All</td> </tr> <tr> <td>11b</td> <td>Normal</td> <td>Link not in training: Send normal pixels</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All	01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All	10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All	11b	Normal	Link not in training: Send normal pixels	All
Value	Name	Description	Project																				
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All																				
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All																				
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All																				
11b	Normal	Link not in training: Send normal pixels	All																				



DPB—DisplayPort B Control Register

27:25	<p>Voltage_swing_level_set</p> <p>Project: All Default Value: 0b</p> <p>These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration.</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0.4V</td> <td>0.4 V</td> <td>All</td> </tr> <tr> <td>001b</td> <td>0.6V</td> <td>0.6 V</td> <td>All</td> </tr> <tr> <td>010b</td> <td>0.8V</td> <td>0.8 V</td> <td>All</td> </tr> <tr> <td>011b</td> <td>1.2V</td> <td>1.2 V</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	000b	0.4V	0.4 V	All	001b	0.6V	0.6 V	All	010b	0.8V	0.8 V	All	011b	1.2V	1.2 V	All	1XXb	Reserved	Reserved	All
Value Name	Description	Project																						
000b	0.4V	0.4 V	All																					
001b	0.6V	0.6 V	All																					
010b	0.8V	0.8 V	All																					
011b	1.2V	1.2 V	All																					
1XXb	Reserved	Reserved	All																					
24:22	<p>Pre-emphasis_level_set</p> <p>Project: All Default Value: 0b</p> <p>These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration.</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>None</td> <td>No pre-emphasis</td> <td>All</td> </tr> <tr> <td>001b</td> <td>3.5dB</td> <td>3.5dB pre-emphasis (1.5x)</td> <td>All</td> </tr> <tr> <td>010b</td> <td>6 dB</td> <td>6dB pre-emphasis (2x)</td> <td>All</td> </tr> <tr> <td>011b</td> <td>9.5 dB</td> <td>9.5dB pre-emphasis (3x)</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	000b	None	No pre-emphasis	All	001b	3.5dB	3.5dB pre-emphasis (1.5x)	All	010b	6 dB	6dB pre-emphasis (2x)	All	011b	9.5 dB	9.5dB pre-emphasis (3x)	All	1XXb	Reserved	Reserved	All
Value Name	Description	Project																						
000b	None	No pre-emphasis	All																					
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All																					
010b	6 dB	6dB pre-emphasis (2x)	All																					
011b	9.5 dB	9.5dB pre-emphasis (3x)	All																					
1XXb	Reserved	Reserved	All																					
21:19	<p>Port_Width_Selection</p> <p>Project: All Default Value: 0b</p> <p>This bit selects the number of lanes to be enabled on the DisplayPort link. Port width change must be done as a part of mode set. Locked once port is enabled. Updates when the port is disabled then re-enabled</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>x1</td> <td>x1 Mode</td> <td>All</td> </tr> <tr> <td>001b</td> <td>x2</td> <td>x2 Mode</td> <td>All</td> </tr> <tr> <td>011b</td> <td>x4</td> <td>x4 Mode</td> <td>All</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	000b	x1	x1 Mode	All	001b	x2	x2 Mode	All	011b	x4	x4 Mode	All	Others	Reserved	Reserved	All				
Value Name	Description	Project																						
000b	x1	x1 Mode	All																					
001b	x2	x2 Mode	All																					
011b	x4	x4 Mode	All																					
Others	Reserved	Reserved	All																					



DPB—DisplayPort B Control Register

18	<p>Enhanced_Framing_Enable Project: All Default Value: 0b This bit selects enhanced framing. Locked once port is enabled. Updates when the port is disabled then re-enabled</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 15%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Enhanced framing disabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enhanced framing enabled</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	0b	Disable	Enhanced framing disabled	All	1b	Enable	Enhanced framing enabled	All
Value Na	me	Description	Project										
0b	Disable	Enhanced framing disabled	All										
1b	Enable	Enhanced framing enabled	All										
17:16	<p>Reserved Project: All Format: MBZ</p>												
15	<p>Port_reversal Project: All Default Value: 0b Enables lane reversal within the port: lane 0 mapped to lane 3, lane 1 mapped to lane 2, etc. Port reversal is not controlled by a strap. Locked once port is enabled. Updates when the port is disabled then re-enabled</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 15%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Reversed</td> <td>Port not reversed</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Reversed</td> <td>Port reversed</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	0b	Not Reversed	Port not reversed	All	1b	Reversed	Port reversed	All
Value Na	me	Description	Project										
0b	Not Reversed	Port not reversed	All										
1b	Reversed	Port reversed	All										
14:8	<p>Reserved Project: All Format: MBZ</p>												
7	<p>Scrambling_Disable Project: All Security: Debug Default Value: 0b This bit disables scrambling for DisplayPort</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 15%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> <td>Scrambling enabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Disable</td> <td>Scrambling disabled</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	0b	Enable	Scrambling enabled	All	1b	Disable	Scrambling disabled	All
Value Na	me	Description	Project										
0b	Enable	Scrambling enabled	All										
1b	Disable	Scrambling disabled	All										
6	<p>Audio_Output_Enable Project: All Default Value: 0b This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to "Normal."</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value Na</th> <th style="width: 15%;">me</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Audio output disabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Audio output enabled</td> <td>All</td> </tr> </tbody> </table>	Value Na	me	Description	Project	0b	Disable	Audio output disabled	All	1b	Enable	Audio output enabled	All
Value Na	me	Description	Project										
0b	Disable	Audio output disabled	All										
1b	Enable	Audio output enabled	All										



DPB—DisplayPort B Control Register																							
5	Reserved																						
4:3	<p>Sync_Polarity Project: All Default Value: 11b VS and HS are active high Indicates the polarity of Hsync and Vsync to be transmitted in MSA</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Low</td> <td>VS and HS are active low (inverted)</td> <td>All</td> </tr> <tr> <td>11b</td> <td>VS Low, HS High</td> <td>VS is active low (inverted), HS is active high</td> <td>All</td> </tr> <tr> <td>11b</td> <td>VS High, HS Low</td> <td>VS is active high, HS is active low (inverted)</td> <td>All</td> </tr> <tr> <td>11b</td> <td>High</td> <td>VS and HS are active high</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	00b	Low	VS and HS are active low (inverted)	All	11b	VS Low, HS High	VS is active low (inverted), HS is active high	All	11b	VS High, HS Low	VS is active high, HS is active low (inverted)	All	11b	High	VS and HS are active high	All
Value	Name	Description	Project																				
00b	Low	VS and HS are active low (inverted)	All																				
11b	VS Low, HS High	VS is active low (inverted), HS is active high	All																				
11b	VS High, HS Low	VS is active high, HS is active low (inverted)	All																				
11b	High	VS and HS are active high	All																				
2	<p>Digital_Display_B_Detected Project: All Access: Read Only Default Value: 0b Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Detected</td> <td>Digital display not detected during initialization</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Detected</td> <td>Digital display detected during initialization</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Not Detected	Digital display not detected during initialization	All	1b	Detected	Digital display detected during initialization	All								
Value	Name	Description	Project																				
0b	Not Detected	Digital display not detected during initialization	All																				
1b	Detected	Digital display detected during initialization	All																				
1:0	Reserved	Project: All	Format: MBZ																				



4.3.2 DPB_AUX_CH_CTL—Display Port B AUX Channel Control

DPB_AUX_CH_CTL—Display Port B AUX Channel Control																					
Register Type: MMIO Address Offset: E4110h Project: All Default Value: 00050000h Access: R/W Size (in bits): 32																					
Bit De	scription																				
31	Send/Busy Project: All Default Value: 0b Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.																				
<table border="1"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">Do not change any fields while Busy bit 31 is asserted.</td> </tr> </tbody> </table>		Programming Notes		Do not change any fields while Busy bit 31 is asserted.																	
Programming Notes																					
Do not change any fields while Busy bit 31 is asserted.																					
30	Done Project: All Access: R/W Clear A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event.																				
29	Interrupt_on_Done Project: All Format: Enable an interrupt in the hotplug status register when the transaction completes or times out.																				
28	Time_out_error Project: All Access: R/W Clear A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event.																				
27:26	Time_out_timer_value Project: All Default Value: 0b The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.																				
<table border="1"> <thead> <tr> <th>Value Na</th> <th>me</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>400us</td> <td>400us</td> <td>All</td> </tr> <tr> <td>01b</td> <td>600us</td> <td>600us</td> <td>All</td> </tr> <tr> <td>10b</td> <td>800us</td> <td>800us</td> <td>All</td> </tr> <tr> <td>11b</td> <td>1600us</td> <td>1600us</td> <td>All</td> </tr> </tbody> </table>		Value Na	me	Description	Project	00b	400us	400us	All	01b	600us	600us	All	10b	800us	800us	All	11b	1600us	1600us	All
Value Na	me	Description	Project																		
00b	400us	400us	All																		
01b	600us	600us	All																		
10b	800us	800us	All																		
11b	1600us	1600us	All																		
25	Receive_error Project: All Access: R/W Clear A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event.																				



DPB_AUX_CH_CTL—Display Port B AUX Channel Control

24:20	<p>Message_Size Project: All Format:</p> <p>This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only when the done bit is set, and if timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size.</p> <p>Reads of this field will give the response message size.</p> <p>The read value will not be valid while Busy bit 31 is asserted.</p> <p>Message sizes of 0 or >20 are not allowed.</p>												
19:16	<p>Precharge_Time Project: All Format:</p> <p>Default Value: 0101b 10us</p> <p>Used to determine the precharge time for the Aux Channel drivers.</p> <p>The value is the number of microseconds times 2 (assuming 2X bit clock divider programmed for 2MHz).</p> <p>Default is 5 decimal which gives 10us of precharge.</p> <p>Example:</p> <p>For 10us precharge, program 5 (10us/2us).</p>												
15	Reserved												
14	<p>Invert_Manchester</p> <p>Project: All</p> <p>Security: Test</p> <p>Default Value: 0b</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Normal</td> <td>Manchester code rising edge mid-clk signifies zero</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Invert</td> <td>Manchester code rising edge mid-clk signifies one</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Normal	Manchester code rising edge mid-clk signifies zero	All	1b	Invert	Manchester code rising edge mid-clk signifies one	All
Value	Name	Description	Project										
0b	Normal	Manchester code rising edge mid-clk signifies zero	All										
1b	Invert	Manchester code rising edge mid-clk signifies one	All										
13	<p>Sync_Only_Clock_Recovery</p> <p>Project: All</p> <p>Security: Test</p> <p>Default Value: 0b</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Sync and Data</td> <td>Recover clock during sync pattern and data phase</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Sync Only</td> <td>Only recover clock during sync pattern</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Sync and Data	Recover clock during sync pattern and data phase	All	1b	Sync Only	Only recover clock during sync pattern	All
Value	Name	Description	Project										
0b	Sync and Data	Recover clock during sync pattern and data phase	All										
1b	Sync Only	Only recover clock during sync pattern	All										



DPB_AUX_CH_CTL—Display Port B AUX Channel Control

12	<p>Disable_De-glitch</p> <p>Project: All Security: Test Default Value: 0b</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: left;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Enable</td> <td>Enable serial input de-glitch logic</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Disable</td> <td>Disable serial input de-glitch logic</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Enable	Enable serial input de-glitch logic	All	1b	Disable	Disable serial input de-glitch logic	All
Value	Name	Description	Project										
0b	Enable	Enable serial input de-glitch logic	All										
1b	Disable	Disable serial input de-glitch logic	All										
11	<p>Double_precharge</p> <p>Project: All Security: Test Default Value: 0b</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: left;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Programmed</td> <td>Precharge time is as programmed</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Doubled</td> <td>Precharge time is doubled</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Programmed	Precharge time is as programmed	All	1b	Doubled	Precharge time is doubled	All
Value	Name	Description	Project										
0b	Programmed	Precharge time is as programmed	All										
1b	Doubled	Precharge time is doubled	All										
10:0	<p>2X_Bit_Clock_divider Project: All Format: 2*U11</p> <p>Used to determine the 2X bit clock the Aux Channel logic runs on.</p> <p>This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). The input clock is the 125mhz rawclk.</p> <p>Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).</p>												



4.3.3 DPB_AUX_CH_DATA—Display Port B AUX Data Registers

DP Aux Ch Data Format	
Project:	All
Bit De	scription
31:0	AUX_CH_DATA Project: All A DWord of the message. Writes give the data to transmit during the transaction. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

DPB_AUX_CH_DATA—Display Port B AUX Data Registers	
Register Type:	MMIO
Address Offset:	E4114h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	5x32
The read value will not be valid while Busy bit 31 is asserted.	
DWord Bit	Description
0	31:0 AUX_CH_DATA1 Project: All Format: DP Aux Ch Data Format
1	31:0 AUX_CH_DATA2 Project: All Format: DP Aux Ch Data Format
2	31:0 AUX_CH_DATA3 Project: All Format: DP Aux Ch Data Format
3	31:0 AUX_CH_DATA4 Project: All Format: DP Aux Ch Data Format
4	31:0 AUX_CH_DATA5 Project: All Format: DP Aux Ch Data Format

]



4.4 DPC Control and Aux Channel

4.4.1 DPC—Display Port C Control Register

DPC—Display Port C Control Register			
Register Type:	MMIO		
Address Offset:	E4200h		
Project:	All		
Default Value:	00000018h		
Access:	R/W Protect		
Size (in bits):	32		
Double Buffer Update Point:	Depends on bit		
Port enable and transcoder select are write protected by Panel Power Sequencer when panel is connected to this port. Please note that DisplayPort C uses the same lanes as HDMI. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously.			
Bit De	scription		
31	DisplayPort_C_Enable Project: All Default Value: 0b See DPB description. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMIC from being enabled on transcoder A.		
	Value Na	me	Description
	0b	Disable	Disable and tristates the Display Port C interface
	1b	Enable	Enable. This bit enables the Display Port C interface
		Project	All
30	Transcoder_Select Project: All Default Value: 0b See DPB description. [DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.		
	Value Na	me	Description
	0b	Transcoder A	Transcoder A
	1b	Transcoder B	Transcoder B
		Project	All



DPC—Display Port C Control Register

29:28	<p>Link_training_pattern_enable</p> <p>Project: All Default Value: 0b</p> <p>These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.</p> <p>When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Pattern 1</td> <td>Pattern 1 enabled: Repetition of D10.2 characters</td> <td>All</td> </tr> <tr> <td>01b</td> <td>Pattern 2</td> <td>Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.</td> <td>All</td> </tr> <tr> <td>10b</td> <td>Idle</td> <td>Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times</td> <td>All</td> </tr> <tr> <td>11b</td> <td>Normal</td> <td>Link not in training: Send normal pixels</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All	01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All	10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All	11b	Normal	Link not in training: Send normal pixels	All				
Value Name	Description	Project																						
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All																					
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All																					
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All																					
11b	Normal	Link not in training: Send normal pixels	All																					
27:25	<p>Voltage_swing_level_set</p> <p>Project: All Default Value: 0b</p> <p>See DPB description.</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0.4V</td> <td>0.4 V</td> <td>All</td> </tr> <tr> <td>001b</td> <td>0.6V</td> <td>0.6 V</td> <td>All</td> </tr> <tr> <td>010b</td> <td>0.8V</td> <td>0.8 V</td> <td>All</td> </tr> <tr> <td>011b</td> <td>1.2V</td> <td>1.2 V</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	000b	0.4V	0.4 V	All	001b	0.6V	0.6 V	All	010b	0.8V	0.8 V	All	011b	1.2V	1.2 V	All	1XXb	Reserved	Reserved	All
Value Name	Description	Project																						
000b	0.4V	0.4 V	All																					
001b	0.6V	0.6 V	All																					
010b	0.8V	0.8 V	All																					
011b	1.2V	1.2 V	All																					
1XXb	Reserved	Reserved	All																					
24:22	<p>Pre-emphasis_level_set</p> <p>Project: All Default Value: 0b</p> <p>See DPB description.</p> <table border="1"> <thead> <tr> <th>Value Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>None</td> <td>No pre-emphasis</td> <td>All</td> </tr> <tr> <td>001b</td> <td>3.5dB</td> <td>3.5dB pre-emphasis (1.5x)</td> <td>All</td> </tr> <tr> <td>010b</td> <td>6 dB</td> <td>6dB pre-emphasis (2x)</td> <td>All</td> </tr> <tr> <td>011b</td> <td>9.5 dB</td> <td>9.5dB pre-emphasis (3x)</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value Name	Description	Project	000b	None	No pre-emphasis	All	001b	3.5dB	3.5dB pre-emphasis (1.5x)	All	010b	6 dB	6dB pre-emphasis (2x)	All	011b	9.5 dB	9.5dB pre-emphasis (3x)	All	1XXb	Reserved	Reserved	All
Value Name	Description	Project																						
000b	None	No pre-emphasis	All																					
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All																					
010b	6 dB	6dB pre-emphasis (2x)	All																					
011b	9.5 dB	9.5dB pre-emphasis (3x)	All																					
1XXb	Reserved	Reserved	All																					



DPC—Display Port C Control Register

21:19	<p>Port_Width_Selection</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>x1</td> <td>x1 Mode</td> <td>All</td> </tr> <tr> <td>001b</td> <td>x2</td> <td>x2 Mode</td> <td>All</td> </tr> <tr> <td>011b</td> <td>x4</td> <td>x4 Mode</td> <td>All</td> </tr> <tr> <td>others</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	000b	x1	x1 Mode	All	001b	x2	x2 Mode	All	011b	x4	x4 Mode	All	others	Reserved	Reserved	All
Value	Name	Description	Project																		
000b	x1	x1 Mode	All																		
001b	x2	x2 Mode	All																		
011b	x4	x4 Mode	All																		
others	Reserved	Reserved	All																		
18	<p>Enhanced_Framing_Enable</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Enhanced framing disabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enhanced framing enabled</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Disable	Enhanced framing disabled	All	1b	Enable	Enhanced framing enabled	All								
Value	Name	Description	Project																		
0b	Disable	Enhanced framing disabled	All																		
1b	Enable	Enhanced framing enabled	All																		
17:16	<p>Reserved Project: All Format: MBZ</p>																				
15	<p>Port_reversal</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Reversed</td> <td>Port not reversed</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Reversed</td> <td>Port reversed</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Not Reversed	Port not reversed	All	1b	Reversed	Port reversed	All								
Value	Name	Description	Project																		
0b	Not Reversed	Port not reversed	All																		
1b	Reversed	Port reversed	All																		
14:8	<p>Reserved Project: All Format: MBZ</p>																				
7	<p>Scrambling_Disable</p> <p>Project: All Security: Debug Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> <td>Scrambling enabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Disable</td> <td>Scrambling disabled</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Enable	Scrambling enabled	All	1b	Disable	Scrambling disabled	All								
Value	Name	Description	Project																		
0b	Enable	Scrambling enabled	All																		
1b	Disable	Scrambling disabled	All																		



DPC—Display Port C Control Register																							
6	<p>Audio_Output_Enable</p> <p>Project: All</p> <p>Default Value: 0b</p> <p>This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to “Normal.”</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> <td>Audio output disabled</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> <td>Audio output enabled</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Disable	Audio output disabled	All	1b	Enable	Audio output enabled	All								
Value	Name	Description	Project																				
0b	Disable	Audio output disabled	All																				
1b	Enable	Audio output enabled	All																				
5	Reserved																						
4:3	<p>Sync_Polarity</p> <p>Project: All</p> <p>Default Value: 11b VS and HS are active high</p> <p>See DPB description.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">Low</td> <td>VS and HS are active low (inverted)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">VS Low, HS High</td> <td>VS is active low (inverted), HS is active high</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">VS High, HS Low</td> <td>VS is active high, HS is active low (inverted)</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">High</td> <td>VS and HS are active high</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>			Value	Name	Description	Project	00b	Low	VS and HS are active low (inverted)	All	11b	VS Low, HS High	VS is active low (inverted), HS is active high	All	11b	VS High, HS Low	VS is active high, HS is active low (inverted)	All	11b	High	VS and HS are active high	All
Value	Name	Description	Project																				
00b	Low	VS and HS are active low (inverted)	All																				
11b	VS Low, HS High	VS is active low (inverted), HS is active high	All																				
11b	VS High, HS Low	VS is active high, HS is active low (inverted)	All																				
11b	High	VS and HS are active high	All																				
2	<p>Digital_Display_C_Detected</p> <p>Project: All</p> <p>Access: Read Only</p> <p>Default Value: 0b</p> <p>Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> <th style="text-align: center;">Project</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Not Detected</td> <td>Digital display not detected during initialization</td> <td style="text-align: center;">All</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Detected</td> <td>Digital display detected during initialization</td> <td style="text-align: center;">All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Not Detected	Digital display not detected during initialization	All	1b	Detected	Digital display detected during initialization	All								
Value	Name	Description	Project																				
0b	Not Detected	Digital display not detected during initialization	All																				
1b	Detected	Digital display detected during initialization	All																				
1:0	<p>Reserved Project: All Format: MBZ</p>																						



4.4.2 DPC_AUX_CH_CTL—Display Port C AUX Channel Control

DPC_AUX_CH_CTL—Display Port C AUX Channel Control																							
Register Type: MMIO Address Offset: E4210h Project: All Default Value: 00050000h Access: R/W Size (in bits): 32																							
Bit De	scription																						
31	Send/Busy Project: All Default Value: 0b See DPB description. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">Do not change any fields while Busy bit 31 is asserted.</td> </tr> </tbody> </table>			Programming Notes		Do not change any fields while Busy bit 31 is asserted.																	
Programming Notes																							
Do not change any fields while Busy bit 31 is asserted.																							
30	Done	Project: All	Access: R/W Clear																				
See DPB description.																							
29	Interrupt_on_Done	Project: All	Format:																				
See DPB description.																							
28	Time_out_error	Project: All	Access: R/W Clear																				
See DPB description.																							
27:26	Time_out_timer_value Project: All Default Value: 0b See DPB description. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th>Value Name</th> <th>me</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>400us</td> <td>400us</td> <td>All</td> </tr> <tr> <td>01b</td> <td>600us</td> <td>600us</td> <td>All</td> </tr> <tr> <td>10b</td> <td>800us</td> <td>800us</td> <td>All</td> </tr> <tr> <td>11b</td> <td>1600us</td> <td>1600us</td> <td>All</td> </tr> </tbody> </table>			Value Name	me	Description	Project	00b	400us	400us	All	01b	600us	600us	All	10b	800us	800us	All	11b	1600us	1600us	All
Value Name	me	Description	Project																				
00b	400us	400us	All																				
01b	600us	600us	All																				
10b	800us	800us	All																				
11b	1600us	1600us	All																				
25	Receive_error	Project: All	Access: R/W Clear																				
See DPB description.																							
24:20	Message_Size	Project: All	Format:																				
See DPB description.																							



DPC_AUX_CH_CTL—Display Port C AUX Channel Control															
19:16	Precharge_Time	Project: All Format: 5 decimal which gives 10us of precharge													
	Default Value: 0101b See DPB description.														
15	Reserved														
14	Invert_Manchester	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Zero</td> <td>Manchester code rising edge mid-clk signifies zero</td> <td>All</td> </tr> <tr> <td>1b</td> <td>One</td> <td>Manchester code rising edge mid-clk signifies one</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Zero	Manchester code rising edge mid-clk signifies zero	All	1b	One	Manchester code rising edge mid-clk signifies one	All
Value	Name	Description	Project												
0b	Zero	Manchester code rising edge mid-clk signifies zero	All												
1b	One	Manchester code rising edge mid-clk signifies one	All												
13	Sync_Only_Clock_Recovery	Project: All Security: Test Default Value: 0b													
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Value	Name	Description	Project												
0b	Sync and Data	Recover clock during sync pattern and data phase	All												
1b	Sync Only	Only recover clock during sync pattern	All												
12	Disable_De-glitch	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> <td>Enable serial input de-glitch logic</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Disable</td> <td>Disable serial input de-glitch logic</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Enable	Enable serial input de-glitch logic	All	1b	Disable	Disable serial input de-glitch logic	All
Value	Name	Description	Project												
0b	Enable	Enable serial input de-glitch logic	All												
1b	Disable	Disable serial input de-glitch logic	All												
11	Double_precharge	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Programmed</td> <td>Precharge time is as programmed</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Doubled</td> <td>Precharge time is doubled</td> <td>All</td> </tr> </tbody> </table>			Value	Name	Description	Project	0b	Programmed	Precharge time is as programmed	All	1b	Doubled	Precharge time is doubled	All
Value	Name	Description	Project												
0b	Programmed	Precharge time is as programmed	All												
1b	Doubled	Precharge time is doubled	All												
10:0	2X_Bit_Clock_divider	Project: All Format: 2*U11													
	See DPB description.														



4.4.3 DPC_AUX_CH_DATA—Display Port C AUX Data Registers

DPC_AUX_CH_DATA—Display Port C AUX Data Registers				
Register Type: MMIO				
Address Offset: E4214h				
Project: All				
Default Value: 00000000h;				
Access: R/W				
Size (in bits): 5x32				
The read value will not be valid while Busy bit 31 is asserted.				
DWord Bit		Description		
0	31:0	AUX_CH_DATA1	Project: All	Format: DP Aux Ch Data Format
1	31:0	AUX_CH_DATA2	Project: All	Format: DP Aux Ch Data Format
2	31:0	AUX_CH_DATA3	Project: All	Format: DP Aux Ch Data Format
3	31:0	AUX_CH_DATA4	Project: All	Format: DP Aux Ch Data Format
4	31:0	AUX_CH_DATA5	Project: All	Format: DP Aux Ch Data Format



4.5 DPD Control and Aux Channel

4.5.1 DPD—DisplayPort D Control Register

DPD—DisplayPort D Control Register			
Register Type:	MMIO		
Address Offset:	E4300h		
Project:	All		
Default Value:	00000018h		
Access:	R/W Protect		
Size (in bits):	32		
Double Buffer Update Point:	Depends on bit		
Port enable and transcoder select are write protected by Panel Power Sequencer when panel is connected to this port. Please note that DisplayPort D uses the same lanes as HDMID. Therefore HDMID and DisplayPort D cannot be enabled simultaneously.			
Bit De	scription		
31	DisplayPort_D_Enable Project: All Default Value: 0b See DPB description. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to '0' after disabling the port. This is workaround for hardware issue where the transcoder select set to '1' will prevent HDMID from being enabled on transcoder A.		
	Value Na	me	Description
	0b	Disable	Disable and tristates the Display Port D interface
	1b	Enable	Enable. This bit enables the Display Port D interface
			Project
			All
			All



DPD—DisplayPort D Control Register

30	<p>Transcoder_Select Project: All Default Value: 0b See DPB description.</p> <p>[DevIBX] Writing to this bit only takes effect when port is enabled. Due to hardware issue it is required that this bit be cleared when port is disabled. To clear this bit software must temporarily enable this port on transcoder A.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Transcoder A</td> <td>Transcoder A</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Transcoder B</td> <td>Transcoder B</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Transcoder A	Transcoder A	All	1b	Transcoder B	Transcoder B	All												
Value	Name	Description	Project																						
0b	Transcoder A	Transcoder A	All																						
1b	Transcoder B	Transcoder B	All																						
29:28	<p>Link_training_pattern_enable Project: All Default Value: 0b</p> <p>These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.</p> <p>When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Pattern 1</td> <td>Pattern 1 enabled: Repetition of D10.2 characters</td> <td>All</td> </tr> <tr> <td>01b</td> <td>Pattern 2</td> <td>Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.</td> <td>All</td> </tr> <tr> <td>10b</td> <td>Idle</td> <td>Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times</td> <td>All</td> </tr> <tr> <td>11b</td> <td>Normal</td> <td>Link not in training: Send normal pixels</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All	01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All	10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All	11b	Normal	Link not in training: Send normal pixels	All				
Value	Name	Description	Project																						
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All																						
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All																						
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All																						
11b	Normal	Link not in training: Send normal pixels	All																						
27:25	<p>Voltage_swing_level_set Project: All Default Value: 0b See DPB description.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 55%;">Description</th> <th style="width: 15%;">Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0.4V</td> <td>0.4 V</td> <td>All</td> </tr> <tr> <td>001b</td> <td>0.6V</td> <td>0.6 V</td> <td>All</td> </tr> <tr> <td>010b</td> <td>0.8V</td> <td>0.8 V</td> <td>All</td> </tr> <tr> <td>011b</td> <td>1.2V</td> <td>1.2 V</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	000b	0.4V	0.4 V	All	001b	0.6V	0.6 V	All	010b	0.8V	0.8 V	All	011b	1.2V	1.2 V	All	1XXb	Reserved	Reserved	All
Value	Name	Description	Project																						
000b	0.4V	0.4 V	All																						
001b	0.6V	0.6 V	All																						
010b	0.8V	0.8 V	All																						
011b	1.2V	1.2 V	All																						
1XXb	Reserved	Reserved	All																						



DPD—DisplayPort D Control Register

24:22	<p>Pre-emphasis_level_set</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>None</td> <td>No pre-emphasis</td> <td>All</td> </tr> <tr> <td>001b</td> <td>3.5dB</td> <td>3.5dB pre-emphasis (1.5x)</td> <td>All</td> </tr> <tr> <td>010b</td> <td>6 dB</td> <td>6dB pre-emphasis (2x)</td> <td>All</td> </tr> <tr> <td>011b</td> <td>9.5 dB</td> <td>9.5dB pre-emphasis (3x)</td> <td>All</td> </tr> <tr> <td>1XXb</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	000b	None	No pre-emphasis	All	001b	3.5dB	3.5dB pre-emphasis (1.5x)	All	010b	6 dB	6dB pre-emphasis (2x)	All	011b	9.5 dB	9.5dB pre-emphasis (3x)	All	1XXb	Reserved	Reserved	All
Value	Name	Description	Project																						
000b	None	No pre-emphasis	All																						
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All																						
010b	6 dB	6dB pre-emphasis (2x)	All																						
011b	9.5 dB	9.5dB pre-emphasis (3x)	All																						
1XXb	Reserved	Reserved	All																						
21:19	<p>Port_Width_Selection</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>x1</td> <td>x1 Mode</td> <td>All</td> </tr> <tr> <td>001b</td> <td>x2</td> <td>x2 Mode</td> <td>All</td> </tr> <tr> <td>011b</td> <td>x4</td> <td>x4 Mode</td> <td>All</td> </tr> <tr> <td>others</td> <td>Reserved</td> <td>Reserved</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	000b	x1	x1 Mode	All	001b	x2	x2 Mode	All	011b	x4	x4 Mode	All	others	Reserved	Reserved	All				
Value	Name	Description	Project																						
000b	x1	x1 Mode	All																						
001b	x2	x2 Mode	All																						
011b	x4	x4 Mode	All																						
others	Reserved	Reserved	All																						
18	<p>Enhanced_Framing_Enable</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Enhanced framing disabled</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enhanced framing enabled</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Disable	Enhanced framing disabled	All	1b	Enable	Enhanced framing enabled	All												
Value	Name	Description	Project																						
0b	Disable	Enhanced framing disabled	All																						
1b	Enable	Enhanced framing enabled	All																						
17:16	<p>Reserved Project: All Format: MBZ</p>																								
15	<p>Port_reversal</p> <p>Project: All Default Value: 0b See DPB description.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Reversed</td> <td>Port not reversed</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Reversed</td> <td>Port reversed</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Not Reversed	Port not reversed	All	1b	Reversed	Port reversed	All												
Value	Name	Description	Project																						
0b	Not Reversed	Port not reversed	All																						
1b	Reversed	Port reversed	All																						



DPD—DisplayPort D Control Register			
14:8	Reserved	Project: All	Format: MBZ
7	Scrambling_Disable Project: All Security: Debug Default Value: 0b See DPB description.		
	Value Na	me	Description
	0b	Enable	Scrambling enabled
	1b	Disable	Scrambling disabled
6	Audio_Output_Enable Project: All Default Value: 0b This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to "Normal."		
	Value Na	me	Description
	0b	Disable	Audio output disabled
	1b	Enable	Audio output enabled
5	Reserved		
4:3	Sync_Polarity Project: All Default Value: 11b VS and HS are active high See DPB description.		
	Value Na	me	Description
	00b	Low	VS and HS are active low (inverted)
	11b	VS Low, HS High	VS is active low (inverted), HS is active high
	11b	VS High, HS Low	VS is active high, HS is active low (inverted)
	11b	High	VS and HS are active high



DPD—DisplayPort D Control Register

2	Digital_Display_D_Detected Project: All Access: Read Only Default Value: 0b Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 5 (port D) data line at boot.		
	Value Name	Description	Project
	0b	Not Detected	Digital display not detected during initialization
	1b	Detected	Digital display detected during initialization
1:0	Reserved Project: All		Format: MBZ



4.5.2 DPD_AUX_CH_CTL—Display Port D AUX Channel Control

DPD_AUX_CH_CTL—Display Port D AUX Channel Control																							
Register Type: MMIO Address Offset: E4310h Project: All Default Value: 00050000h Access: R/W Size (in bits): 32																							
Bit De	scription																						
31	Send/Busy Project: All Default Value: 0b See DPB description. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">Do not change any fields while Busy bit 31 is asserted.</td> </tr> </tbody> </table>			Programming Notes		Do not change any fields while Busy bit 31 is asserted.																	
Programming Notes																							
Do not change any fields while Busy bit 31 is asserted.																							
30	Done	Project: All	Access: R/W Clear																				
See DPB description.																							
29	Interrupt_on_Done	Project: All	Format:																				
See DPB description.																							
28	Time_out_error	Project: All	Access: R/W Clear																				
See DPB description.																							
27:26	Time_out_timer_value Project: All Default Value: 0b See DPB description. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th>Value Na</th> <th>me</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>400us</td> <td>400us</td> <td>All</td> </tr> <tr> <td>01b</td> <td>600us</td> <td>600us</td> <td>All</td> </tr> <tr> <td>10b</td> <td>800us</td> <td>800us</td> <td>All</td> </tr> <tr> <td>11b</td> <td>1600us</td> <td>1600us</td> <td>All</td> </tr> </tbody> </table>			Value Na	me	Description	Project	00b	400us	400us	All	01b	600us	600us	All	10b	800us	800us	All	11b	1600us	1600us	All
Value Na	me	Description	Project																				
00b	400us	400us	All																				
01b	600us	600us	All																				
10b	800us	800us	All																				
11b	1600us	1600us	All																				
25	Receive_error	Project: All	Access: R/W Clear																				
See DPB description.																							
24:20	Message_Size	Project: All	Format:																				
See DPB description.																							



DPD_AUX_CH_CTL—Display Port D AUX Channel Control															
19:16	Precharge_Time	Project: All Format: 5 decimal which gives 10us of precharge													
	Default Value: 0101b See DPB description.														
15	Reserved														
14	Invert_Manchester	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Zero</td> <td>Manchester code rising edge mid-clk signifies zero</td> <td>All</td> </tr> <tr> <td>1b</td> <td>One</td> <td>Manchester code rising edge mid-clk signifies one</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Zero	Manchester code rising edge mid-clk signifies zero	All	1b	One	Manchester code rising edge mid-clk signifies one	All		
Value	Name	Description	Project												
0b	Zero	Manchester code rising edge mid-clk signifies zero	All												
1b	One	Manchester code rising edge mid-clk signifies one	All												
13	Sync_Only_Clock_Recovery	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Sync and Data</td> <td>Recover clock during sync pattern and data phase</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Sync Only</td> <td>Only recover clock during sync pattern</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Sync and Data	Recover clock during sync pattern and data phase	All	1b	Sync Only	Only recover clock during sync pattern	All		
Value	Name	Description	Project												
0b	Sync and Data	Recover clock during sync pattern and data phase	All												
1b	Sync Only	Only recover clock during sync pattern	All												
12	Disable_De-glitch	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> <td>Enable serial input de-glitch logic</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Disable</td> <td>Disable serial input de-glitch logic</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Enable	Enable serial input de-glitch logic	All	1b	Disable	Disable serial input de-glitch logic	All		
Value	Name	Description	Project												
0b	Enable	Enable serial input de-glitch logic	All												
1b	Disable	Disable serial input de-glitch logic	All												
11	Double_precharge	Project: All Security: Test Default Value: 0b													
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Programmed</td> <td>Precharge time is as programmed</td> <td>All</td> </tr> <tr> <td>1b</td> <td>Doubled</td> <td>Precharge time is doubled</td> <td>All</td> </tr> </tbody> </table>	Value	Name	Description	Project	0b	Programmed	Precharge time is as programmed	All	1b	Doubled	Precharge time is doubled	All		
Value	Name	Description	Project												
0b	Programmed	Precharge time is as programmed	All												
1b	Doubled	Precharge time is doubled	All												
10:0	2X_Bit_Clock_divider	Project: All Format: 2*U11													
	See DPB description.														



4.5.3 DPD_AUX_CH_DATA—Display Port D AUX Data Registers

DPD_AUX_CH_DATA—Display Port D AUX Data Registers				
Register Type: MMIO				
Address Offset: E4314h				
Project: All				
Default Value: 00000000h;				
Access: R/W				
Size (in bits): 5x32				
The read value will not be valid while Busy bit 31 is asserted.				
DWord Bit		Description		
0	31:0	AUX_CH_DATA1	Project: All	Format: DP Aux Ch Data Format
1	31:0	AUX_CH_DATA2	Project: All	Format: DP Aux Ch Data Format
2	31:0	AUX_CH_DATA3	Project: All	Format: DP Aux Ch Data Format
3	31:0	AUX_CH_DATA4	Project: All	Format: DP Aux Ch Data Format
4	31:0	AUX_CH_DATA5	Project: All	Format: DP Aux Ch Data Format



4.6 DP_BUFTRANS—DisplayPort Buffer Translation

DisplayPort Buffer Translation Format			
Project:		All	
Default Value:		00000000h	
Bit De	scription		
31:28	Reserved	Project: All	Format: MBZ
27:19	OE These bits select the OE vswing level	Project: All	Range: 0..511
18:17	Reserved	Project: All	Format: MBZ
16:12	Pre_Emphasis These bits select the pre-emphasis level	Project: All	Range: 0..31
11:10	Reserved	Project: All	Format: MBZ
9:6	P_current_drive These bits select the P current drive value	Project: All	Range: 0..15
5:4	Reserved	Project: All	Format: MBZ
3:0	N_current_drive These bits select the N current drive value	Project: All	Range: 0..15

The register defaults for B0 silicon was provided by EV team (2/09). These MUST be programmed by software before enabling DisplayPort the first time. They only need to be programmed once after power on.



10/6/09: L3 0dB setting has been revised to pass compliance testing

DP mode		Offset	Value
L1	0dB	0xE4F00	0x0100030C
L1	3.5dB	0xE4F04	0x00B8230C
L1	6dB	0xE4F08	0x06F8930C
L1	9.5dB	0xE4F0C	0x09F8E38E
L2	0dB	0xE4F10	0x00B8030C
L2	3.5dB	0xE4F14	0x0B78830C
L2	6dB	0xE4F18	0xFF8D3CF
L3	0dB	0xE4F1C	0x01E8030C
L3	3.5dB	0xE4F20	0xFF863CF
L4	0 dB	0xE4F24	0xFF803CF

Vswing	0dB pre-emphasis	3.5dB pre-emphasis	6dB pre-emphasis	9.5dB pre-emphasis
400mV	E4F00	E4F04	E4F08	E4F0C
600mV	E4F10	E4F14	E4F18	Not supported
800mV	E4F1C	E4F20	Not supported	Not supported
1200mV	E4F24	Not supported	Not supported	Not supported



DP_BUFTRANS—DisplayPort Buffer Translation

Register Type: MMIO
Address Offset: E4F00h
Project: DevlBX-B+
Default Value: 0100038Eh; 00B8338Eh; 0178838Eh; 09F8E38Eh; 00B8038Eh; 0978838Eh; 09F8B38E; 0178038Eh; 09F8638Eh; 09F8038Eh
Access: Write Only
Size (in bits): 10x32

These registers define current drive, pre-emphasis and voltage swing buffer programming required for the different voltage swing and pre-emphasis settings in the DisplayPort Control.

DWord Bit		Description		
0	31:0	Voltage_swing_400mV_and_Pre-emphasis_0.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
1	31:0	Voltage_swing_400mV_and_Pre-emphasis_3.5dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
2	31:0	Voltage_swing_400mV_and_Pre-emphasis_6.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
3	31:0	Voltage_swing_400mV_and_Pre-emphasis_9.5dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
4	31:0	Voltage_swing_600mV_and_Pre-emphasis_0.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
5	31:0	Voltage_swing_600mV_and_Pre-emphasis_3.5dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
6	31:0	Voltage_swing_600mV_and_Pre-emphasis_6.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
7	31:0	Voltage_swing_800mV_and_Pre-emphasis_0.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
8	31:0	Voltage_swing_800mV_and_Pre-emphasis_3.5dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	
9	31:0	Voltage_swing_1200mV_and_Pre-emphasis_0.0dB	Project:	All
		Format: DisplayPort Buffer Translation Format	See Description Above	



5. South AFE Registers (FC000h– FFFFFFh)

This topic is documented separately