



Intel[®] OpenSource HD Graphics Programmer's Reference Manual (PRM) Volume 3 Part 1: VGA and Extended VGA Registers (Ivy Bridge)

For the 2012 Intel[®] Core[™] Processor Family

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1. VGA and Extended VGA Registers

This section describes the registers and the functional operation notations for the observable registers in the VGA section. This functionality is provided as a means for support of legacy applications and operating systems. It is important to note that these registers will in general have the desired effects only when running VGA display modes.

The main exceptions to this are the palette interface which will allow real mode DOS applications and full screen VGA applications under an OS control running in high resolution (non-VGA) modes to access the palette through the VGA register mechanisms and the use of the ST01 status bits that determine when the VGA enters display enable and sync periods. Other exceptions include the register bits that control the memory accesses through the A000:0000 and B000:0000 memory segments which would get used during operating system emulation of VGA for “DOS box” applications. Some of the functions of the VGA are enabled or defeated through the programming of the VGA control register bits that are located in the MMIO register space.

Given the legacy nature of this function, it has been adapted to the changing environment that it must operate within. The three most notable changes were the addition of high resolution display mode support, new operating system support, and the use of fixed resolution display devices (such as LCD panels). Additional control bits in the PCI Config space will affect the ability to access the registers and memory aperture associated with VGA.

Mode of Operation	VGA Disable	VGA Display	VGA Registers	Palette (VGA)	VGA Memory	VGA Banking
VGA DOS	No	Yes	Yes	Yes	Yes	No
HiRes DOS	Yes	No	Yes	Yes	No	Yes
Fullscreen DOS	Yes/No	No/Yes	Yes	Yes	Yes	Yes
DOS Emulation	Yes	No	Yes	Yes	Yes	Yes

VGA Display Mode	Dot Clock Select	Dot Clock Range	132 Column Text Support	9-Dot Disable Support	Main Use
Native	VGA Clock Select	25/28 MHz	No	No	Analog CRT (VGA connector)
Centered	Fixed at display Requirements	Product Specific	No	Yes	Digital Display
Upper Left Corner	Fixed at display Requirements	Product Specific	No	Yes	Internal Panel

Native, Centered, and Upper Left Corner support varies from product to product.

Even in the native VGA display operational modes, not all combinations of bit settings result in functional operating modes. VGA display modes have the restriction that they can be used only when all other display planes are disabled.

These registers are accessed via I/O space. The I/O space resides in the PCI compatibility hole and uses only the addresses that were part of the original VGA I/O space (which includes EGA and MDA emulation). Accesses to the VGA I/O addresses are steered to the proper bus and rely on proper setup of bridge registers. Extended VGA registers such as GR10 and GR11 use additional indexes for the already



defined I/O addresses. VGA register accesses are allowed as 8 or 16 bit naturally aligned transactions only. Word transactions must have the least significant bit of the address set to zero. DWORD I/O operations should not be performed on these registers.

Some products may support access to these registers through MMIO. The access method varies and is documented elsewhere.

1.1 General Control and Status Registers

The setup, enable, and general registers are all directly accessible by the CPU. A sub indexing scheme is not used to read from and write to these registers.

Name	Function	Read		Write	
		I/O	Memory Offset	I/O	Memory Offset
ST00	VGA Input Status Register 0	3C2h	3C2h	--	--
ST01	VGA Input Status Register 1	3BAh/3DAh ¹	3BAh/3DAh ¹	--	--
FCR	VGA Feature Control Register	3CAh	3CAh	3BAh/3DAh ¹	3BAh/3DAh ¹
MSR	VGA Miscellaneous Output Register	3CCh	3CCh	3C2h	3C2h

Note:¹ The address selection for ST01 reads and FCR writes is dependent on CGA or MDA emulation mode as selected via the MSR register.

Various bits in these registers provide control over and the real-time status of the horizontal sync signal, the horizontal retrace interval, the vertical sync signal, and the vertical retrace interval. The horizontal retrace interval is the period during the drawing of each scan line containing active video data, when the active video data is not being displayed. This period includes the horizontal front and back porches, and the horizontal sync pulse. The horizontal retrace interval is always longer than the horizontal sync pulse. The vertical retrace interval is the period during which the scan lines not containing active video data are drawn. This includes the vertical front porch, back porch, and the vertical sync pulse. The vertical retrace interval is normally longer than the vertical sync pulse.

Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. In the EGA graphics system (and the ones that preceded it, including MDA and CGA), it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer in while accessing pixel data needed to draw pixels on the display. This resulted in either “snow” or a flickering display.



1.1.1 ST00 - Input Status 0

I/O (and Memory Offset) Address:3C2h

Default:00h

Attributes:Read Only

7	6	5	4	3	2	1	0
CRT Interrupt	Reserved (00)		RGB Cmp / Sen	Reserved (0000)			

Bit	Descriptions
7	<p>CRT Interrupt Pending. This bit is here for EGA compatibility and will always return zero. Note that the generation of interrupts was originally enabled, through bits [4,5] of the Vertical Retrace End Register (CR11). This ability to generate interrupts at the start of the vertical retrace interval is a feature that is typically unused by DOS software and therefore is only supported through other means for use under a operating system support.</p> <p>0 = CRT (vertical retrace interval) interrupt is not pending. 1 = CRT (vertical retrace interval) interrupt is pending</p>
6:5	Reserved. Read as 0s.
4	<p>RGB Comparator / Sense. This bit is here for compatibility and will always return one. Monitor detection must be done be done through the programming of registers in the MMIO space.</p> <p>0 = Below threshold 1 = Above threshold</p>
3:0	Reserved. Read as 0s.

1.1.2 ST01 - Input Status 1

I/O (and Memory Offset) Address:3BAh/3DAh

Default:00h

Attributes:Read Only

The address selection is dependent on CGA or MDA emulation mode as selected via the MSR register.

7	6	5	4	3	2	1	0
Reserved (0)	Reserved (0)	Video Feedback	Vertical Retrace	Reserved (00)	Display Enable		

Bit	Descriptions
7	Reserved (as per VGA specification). Read as 0s.
6	Reserved. Read as 0.
5:4	<p>Video Feedback 1, 0. These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They</p>



Bit	Descriptions
	exist for EGA compatibility.
3	<p>Vertical Retrace/Video.</p> <p>0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place).</p> <p>1 = VSYNC active (Indicates that a vertical retrace interval is taking place).</p> <p>Note:</p> <p>VGA pixel generation is not locked to the display output but is loosely coupled. A VSYNC indication may not occur during the actual VSYNC going to the display but during the VSYNC that is generated as part of the VGA pixel generation. The exact relationship will vary with the VGA display operational mode. This status bit will remain active when the VGA is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now incorrectly) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to.</p> <p>Bits 4 and 5 of the Vertical Retrace End Register (CR11) previously could program this bit to generate an interrupt at the start of the vertical retrace interval. This ability to generate interrupts at the start of the vertical retrace interval is a feature that is largely unused by legacy software. Interrupts are not supported through the VGA register bits.</p>
2:1	Reserved. Read as 0s.
0	<p>Display Enable Output. Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This bit was used with the EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to the frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. Those behaviors resulted in either “snow” or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette RAM with the same address on the same clock cycle.</p> <p>This status bit remains active when the VGA display is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now considered incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. When in panel fitting VGA or centered VGA operation, the meaning of these bits will not be consistent with native VGA timings.</p> <p>0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place.</p> <p>1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.</p>



1.1.3 FCR - Feature Control

I/O (and Memory Offset) Address:3BAh/3DAh - Write; 3CAh - Read

Default:00h

Attributes:See Address above

The I/O address used for writes is dependent on CGA or MDA emulation mode as selected via the MSR register. In the original EGA, bits 0 and 1 were used as part of the feature connector interface. Feature connector is not supported in these devices and those bits will always read as zero.

7 4 3 2 0
Reserved (0000) VSYNC Control Reserved (000)

Bit	Descriptions
7:4	Reserved. Read as 0.
3	<p>VSYNC Control. This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin.</p> <p>0 = Was used to set VSYNC output on the VSYNC pin (default).</p> <p>1 = Was used to set the logical 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful.</p>
2:0	Reserved. Read as 0.

1.1.4 MSR - Miscellaneous Output

I/O (and Memory Offset) Address:3C2h - Write; 3CCh - Read

Default:00h

Attributes:See Address above

7	6	5	4	3	2	1	0
VSYNC Polarity	HSYNC Polarity	Page Select	Reserved (0)	Clock Select	Memory Enable	I/O Address	

Bit	Descriptions
7	<p>CRT VSYNC Polarity. This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. Sync polarity was used in VGA to signal the monitor how many lines of active display are being generated.</p> <p>0 = Positive Polarity (default).</p> <p>1 = Negative Polarity.</p>
6	<p>CRT HSYNC Polarity. This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode.</p> <p>0 = Positive Polarity (default).</p>



Bit	Descriptions
	1 = Negative Polarity
5	<p>Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in display memory for CPU access:</p> <p>0 = Upper page (default)</p> <p>1 = Lower page.</p> <p>Selects between two 64KB pages of frame buffer memory during standard VGA odd/even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.</p>
4	Reserved. Read as 0.
3:2	<p>Clock Select. These bits can select the dot clock source for the CRT interface. The bits should be used to select the dot clock in standard native VGA modes only. When in the centering or upper left corner modes, these bits should be set to have no effect on the clock rate. The actual frequencies that these bits select, if they have any affect at all, is programmable through the DPLL MMIO registers.</p> <p>00 = CLK0, 25.175 MHz (for standard VGA modes with 640 pixel (8-dot) horizontal resolution) (default)</p> <p>01 = CLK1, 28.322 MHz. (for standard VGA modes with 720 pixel (9-dot) horizontal resolution)</p> <p>10 = Was used to select an external clock (now unused)</p> <p>11 = Reserved</p>
1	<p>A0000-BFFFFh Memory Access Enable. VGA Compatibility bit enables access to video memory (frame buffer) at A0000-BFFFFh. When disabled, accesses to VGA memory are blocked in this region. This bit is independent of and does not block CPU access to the video linear frame buffer at other addresses.</p> <p>0 = Prevent CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture (default).</p> <p>1 = Allow CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture. This memory must be mapped as UC by the CPU.</p>
0	<p>I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will "ignore" 3Bx for color configuration or 3Dx for monochrome.</p> <p>Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA.</p> <p>0 = Select 3Bxh I/O address (MDA emulation) (default).</p> <p>1 = Select 3Dxh I/O address (CGA emulation).</p>

Note: In standard VGA modes using the analog VGA connector, bits 7 and 6 indicate which of the three standard VGA vertical resolutions the standard VGA display should use. Extended modes, including those with a vertical resolution of 480 scan lines, may use a setting of 0 for both of these bits. Different connector standards and timing standards specify the proper use of sync polarity. This setting was "reserved" in the VGA standard.



Analog CRT Display Sync Polarities

V	H	Display	Horizontal Frequency	Vertical Frequency
P	P	200 Line	15.7 KHz	60 Hz
N	P	350 Line	21.8 KHz	60 Hz
P	N	400 Line	31.5 KHz	70 Hz
N	N	480 Line	31.5 KHz	60 Hz

1.2 Sequencer Registers

The sequencer registers are accessed via either I/O space or Memory space. To access registers the VGA Sequencer Index register (SRX) at I/O address 3C4h (or memory address 3C4h) is written with the index of the desired register. Then the desired register is accessed through the data port for the sequencer registers at I/O address 3C5 (or memory address 3C5).

1.2.1 SRX - Sequencer Index

I/O (and Memory Offset) Address:3C4h

Default:00h

Attributes:Read/Write

7 32 0
Reserved (0000)Sequencer Index

Bit	Description
7:3	Reserved. Read as 0s.
2:0	Sequencer Index. This field contains a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7. Notes: <ul style="list-style-type: none">• SR02 is referred to in the VGA standard as the Map Mask Register. However, the word “map” is used with multiple meanings in the VGA standard and was, therefore, deemed too confusing; hence, the reason for calling it the Plane Mask Register.• SR07 is a standard VGA register that was not documented. It is not a graphics controller extension.



1.2.2 SR00 - Sequencer Reset

I/O (and Memory Offset) Address:3C5h(Index=00h)

Default:00h

Attributes:Read/Write

7 2 1 0
Reserved (000000)ReservedReserved

Bit	Descriptions
7:2	Reserved. Read as 0.
1	Reserved. Reserved for VGA compatibility (was reset).
0	Reserved. Reserved for VGA compatibility. (was reset)

1.2.3 SR01 - Clocking Mode

I/O (and Memory Offset) Address:3C5h (Index=01h)

Default:00h

Attributes:Read/Write

7 6 5 4 3 2 1 0
Reserved (00)Screen OffShift 4Dot Clock DivideShift LoadReserved (0)8/9 Dot Clocks

Bit	Descriptions
7:6	Reserved. Read as 0s.
5	<p>Screen Off.</p> <p>0 = Normal Operation (default).</p> <p>1 = Disables video output (blanks the screen) and turns off display data fetches. Synchronization pulses to the display, however, are maintained. Setting this bit to 1 had been used as a way to more rapidly update and improve CPU access performance to the frame buffer during VGA modes. In non-VGA modes (VGA Disable=1), this bit has no effect. Before the VGA is disabled through the MMIO VGA control register, this bit should be set to stop the memory accesses from the display.</p> <p>Programming Notes: The following sequence must be used when disabling the VGA plane.</p> <ol style="list-style-type: none"> 1. Write SR01 to set bit 5 = 1 to disable video output. 2. Wait for 100us. 3. Disable the VGA plane via Bit 31 of the MMIO VGA control register (location found in the MMIO display register programming specification).
4	<p>Shift 4.</p> <p>0 = Load video shift registers every 1 or 2 character clocks (depending on bit 2 of this register) (default).</p>



1.2.5 SR03 - Character Font

I/O (and Memory Offset) Address:3C5h (index=03h)

Default:00h

Attributes:Read/Write

7	6	5	4	3	2	1	0
Reserved (00)		Char Map A Select (bit 0)	Char Map B Select (bit 0)	Character Map A Select (bits 2 and 1)		Character Map B Select (bits 2 and 1)	

Bit	Descriptions																											
7:6	Reserved. Read as 0s.																											
3:2,5	<p>Character Map Select Bits for Character Map B. These three bits are used to select the character map (character generator tables) to be used as the secondary character set (font). Note that the numbering of the maps is not sequential.</p> <table border="1"> <thead> <tr> <th>Bit [3:2, 5]</th> <th>Map Number</th> <th>Table Location</th> </tr> </thead> <tbody> <tr> <td>00,0</td> <td>0</td> <td>1st 8KB of plane 2 at offset 0 (default)</td> </tr> <tr> <td>00,1</td> <td>4</td> <td>2nd 8KB of plane 2 at offset 8K</td> </tr> <tr> <td>01,0</td> <td>1</td> <td>3rd 8KB of plane 2 at offset 16K</td> </tr> <tr> <td>01,1</td> <td>5</td> <td>4th 8KB of plane 2 at offset 24K</td> </tr> <tr> <td>10,0</td> <td>2</td> <td>5th 8KB of plane 2 at offset 32K</td> </tr> <tr> <td>10,1</td> <td>6</td> <td>6th 8KB of plane 2 at offset 40K</td> </tr> <tr> <td>11,0</td> <td>3</td> <td>7th 8KB of plane 2 at offset 48K</td> </tr> <tr> <td>11,1</td> <td>7</td> <td>8th 8KB of plane 2 at offset 56K</td> </tr> </tbody> </table>	Bit [3:2, 5]	Map Number	Table Location	00,0	0	1st 8KB of plane 2 at offset 0 (default)	00,1	4	2nd 8KB of plane 2 at offset 8K	01,0	1	3rd 8KB of plane 2 at offset 16K	01,1	5	4th 8KB of plane 2 at offset 24K	10,0	2	5th 8KB of plane 2 at offset 32K	10,1	6	6th 8KB of plane 2 at offset 40K	11,0	3	7th 8KB of plane 2 at offset 48K	11,1	7	8th 8KB of plane 2 at offset 56K
Bit [3:2, 5]	Map Number	Table Location																										
00,0	0	1st 8KB of plane 2 at offset 0 (default)																										
00,1	4	2nd 8KB of plane 2 at offset 8K																										
01,0	1	3rd 8KB of plane 2 at offset 16K																										
01,1	5	4th 8KB of plane 2 at offset 24K																										
10,0	2	5th 8KB of plane 2 at offset 32K																										
10,1	6	6th 8KB of plane 2 at offset 40K																										
11,0	3	7th 8KB of plane 2 at offset 48K																										
11,1	7	8th 8KB of plane 2 at offset 56K																										
1:0,4	<p>Character Map Select Bits for Character Map A. These three bits are used to select the character map (character generator tables) to be used as the primary character set (font). Note that the numbering of the maps is not sequential.</p> <table border="1"> <thead> <tr> <th>Bit [1:0,4]</th> <th>Map Number</th> <th>Table Location</th> </tr> </thead> <tbody> <tr> <td>00,0</td> <td>0</td> <td>1st 8KB of plane 2 at offset 0 (default)</td> </tr> <tr> <td>00,1</td> <td>4</td> <td>2nd 8KB of plane 2 at offset 8K</td> </tr> <tr> <td>01,0</td> <td>1</td> <td>3rd 8KB of plane 2 at offset 16K</td> </tr> <tr> <td>01,1</td> <td>5</td> <td>4th 8KB of plane 2 at offset 24K</td> </tr> <tr> <td>10,0</td> <td>2</td> <td>5th 8KB of plane 2 at offset 32K</td> </tr> <tr> <td>10,1</td> <td>6</td> <td>6th 8KB of plane 2 at offset 40K</td> </tr> <tr> <td>11,0</td> <td>3</td> <td>7th 8KB of plane 2 at offset 48K</td> </tr> <tr> <td>11,1</td> <td>7</td> <td>8th 8KB of plane 2 at offset 56K</td> </tr> </tbody> </table>	Bit [1:0,4]	Map Number	Table Location	00,0	0	1st 8KB of plane 2 at offset 0 (default)	00,1	4	2nd 8KB of plane 2 at offset 8K	01,0	1	3rd 8KB of plane 2 at offset 16K	01,1	5	4th 8KB of plane 2 at offset 24K	10,0	2	5th 8KB of plane 2 at offset 32K	10,1	6	6th 8KB of plane 2 at offset 40K	11,0	3	7th 8KB of plane 2 at offset 48K	11,1	7	8th 8KB of plane 2 at offset 56K
Bit [1:0,4]	Map Number	Table Location																										
00,0	0	1st 8KB of plane 2 at offset 0 (default)																										
00,1	4	2nd 8KB of plane 2 at offset 8K																										
01,0	1	3rd 8KB of plane 2 at offset 16K																										
01,1	5	4th 8KB of plane 2 at offset 24K																										
10,0	2	5th 8KB of plane 2 at offset 32K																										
10,1	6	6th 8KB of plane 2 at offset 40K																										
11,0	3	7th 8KB of plane 2 at offset 48K																										
11,1	7	8th 8KB of plane 2 at offset 56K																										

NOTES:

1. In text modes, bit 3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit 3 controls the foreground intensity.
2. Bit 1 of the Memory Mode Register (SR04) must be set to 1 for the character font select function of this register to be active. Otherwise, only character maps 0 and 4 are available.



1.2.6 SR04 - Memory Mode Register

I/O (and Memory Offset) Address:3C5h (index=04h)

Default:00h

Attributes:Read/Write

7	4	3	2	1	0
Reserved (0000)Chain 4Odd/EvenExtended MemoryReserved (0)					

Bit	Description
7:4	Reserved. Read as 0.
3	<p>Chain 4 Mode. The selections made by this bit affect both CPU Read and write accesses to the frame buffer.</p> <p>0 = The manner in which the frame buffer memory is mapped is determined by the setting of bit 2 of this register (default).</p> <p>1 = The frame buffer memory is mapped in such a way that the function of address bits 0 and 1 are altered so that they select planes 0 through 3. This setting is used in mode x13 to allow all four planes to be accessed via sequential addresses.</p>
2	<p>Odd/Even Mode. Bit 3 of this register must be set to 0 for this bit to be effective. The selections made by this bit affect only non-paged CPU accesses to the frame buffer through the VGA aperture.</p> <p>0 = The frame buffer memory is mapped in such a way that the function of address bit 0 such that even addresses select planes 0 and 2 and odd addresses select planes 1 and 3 (default).</p> <p>1 = Addresses sequentially access data within a bit map, and the choice of which map is accessed is made according to the value of the Plane Mask Register (SR02).</p>
1	<p>Extended Memory Enable. This bit must be set to 1 to enable the selection and use of character maps in plane 2 via the Character Map Select Register (SR03).</p> <p>0 = Disable CPU accesses to more than the first 64KB of VGA standard memory (default).</p> <p>1 = Enable CPU accesses to the rest of the 256KB total VGA memory beyond the first 64KB.</p>
0	Reserved. Read as 0.

1.2.7 SR07 - Horizontal Character Counter Reset

I/O (and Memory Offset) Address:3C5h (index=07h)

Default:00h

Attributes:Read/Write

For standard VGAs, writing this register (with any data) causes the horizontal character counter to be held in reset (the character counter output will remain 0). It remained in reset until a write occurred to any other sequencer register location with SRX set to an index of 0 through 6. In this implementation that sequence has no such special effect.

The vertical line counter is clocked by a signal derived from the horizontal display enable (which does not occur if the horizontal counter is held in reset). Therefore, if a write occurs to this register during the vertical retrace interval, both the horizontal and vertical counters will be set to 0. A write to any other



Bit	Description
	Mode 3, all CPU data written to the frame buffer is rotated, then logically ANDed with the contents of the Bit Mask Register (GR08), and then treated as the addressed data's bit mask, while value of these four bits of this register are treated as the color value.

1.3.3 GR01 - Enable Set/Reset Register

I/O (and Memory Offset) Address:3CFh (Index=01h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7	4	3	2	1	0
Reserved (0000)	Enable	Enable	Enable	Enable	Enable
	Set/ Reset				
	Plane 3	Plane 2	Plane 1	Plane 0	

Bit	Description
7:4	Reserved. Read as 0.
3:0	<p>Enable Set/Reset Plane [3:0].</p> <p>This register works in conjunction with the Set/Reset Register (GR00). The Write Mode bits (bits 0 and 1) must be set for Write Mode 0 for this register to have any effect.</p> <p>0 = The corresponding memory plane can be read from or written to by the CPU without any special bitwise operations taking place.</p> <p>1 = The corresponding memory plane is set to 0 or 1 as specified in the Set/Reset Register (GR00).</p>

1.3.4 GR02 - Color Compare Register

I/O (and Memory Offset) Address:3CFh (Index=02h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7	4	3	2	1	0
Reserved (0000)	Color Compare				
	Plane	Plane	Plane	Plane	
	3	2	1	0	

Bit	Description
7:4	Reserved. Read as 0.
3:0	<p>Color Compare Plane [3:0]. When the Read Mode bit (bit 3) of the Graphics Mode Register (GR05) is set to select Read Mode 1, all 8 bits of each byte of each of the 4 memory planes of the frame buffer corresponding to the address from which a CPU read access is being performed are compared to the corresponding bits in this register (if the corresponding bit in the Color Don't Care Register (GR07) is set to 1).</p> <p>The value that the CPU receives from the read access is an 8-bit value that shows the result of this comparison, wherein value of 1 in a given bit position indicates that all of the corresponding bits in the bytes across all of the memory planes that were included in the comparison had the same value as their memory plane's respective bits in this register.</p>



1.3.5 GR03 - Data Rotate Register

I/O (and Memory Offset) Address:3CFh (Index=03h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7 54 32 0
ReservedFunction SelectRotate Count

Bit	Description
7:5	Reserved. Read as 0.
4:3	<p>Function Select. These bits specify the logical function (if any) to be performed on data that is meant to be written to the frame buffer (using the contents of the memory read latch) just before it is actually stored in the frame buffer at the intended address location.</p> <p>00 = Data being written to the frame buffer remains unchanged, and is simply stored in the frame buffer.</p> <p>01 = Data being written to the frame buffer is logically ANDed with the data in the memory read latch before it is actually stored in the frame buffer.</p> <p>10 = Data being written to the frame buffer is logically ORed with the data in the memory read latch before it is actually stored in the frame buffer.</p> <p>11 = Data being written to the frame buffer is logically XORed with the data in the memory read latch before it is actually stored in the frame buffer.</p>
2:0	<p>Rotate Count. These bits specify the number of bits to the right to rotate any data that is meant to be written to the frame buffer just before it is actually stored in the frame buffer at the intended address location.</p>

1.3.6 GR04 - Read Plane Select Register

I/O (and Memory Offset) Address:3CFh (Index=04h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7 21 0
Reserved (000000)Read Plane Select

Bit	Description
7:2	Reserved. Read as 0.
1:0	<p>Read Plane Select. These two bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even Mode, bit 0 of this register is ignored. In Chain 4 Mode, both bits 1 and 0 of this register are ignored. The four memory planes are selected as follows:</p> <p>00 = Plane 0</p> <p>01 = Plane 1</p> <p>10 = Plane 2</p>



Bit	Description
	<p>11 = Plane 3</p> <p>These two bits also select which of the four memory read latches may be read via the Memory read Latch Data Register (CR22). The choice of memory read latch corresponds to the choice of plane specified in the table above. The Memory Read Latch Data register and this additional function served by 2 bits are features of the VGA standard that were never documented.</p>

1.3.7 GR05 - Graphics Mode Register

I/O (and Memory Offset) Address:3CFh (Index=05h)

Default:0UUU U0UUb (U=Undefined)

Attributes:Read/Write

7 6 5 4 3 2 1 0
 Reserved (0)Shift Register ControlOdd/EvenRead ModeReservedWrite Mode

Bit	Description																																																																																	
7	Reserved. Read as 0.																																																																																	
6:5	<p>Shift Register Control. In standard VGA modes, pixel data is transferred from the 4 graphics memory planes to the palette via a set of 4 serial output bits. These 2 bits of this register control the format in which data in the 4 memory planes is serialized for these transfers to the palette.</p> <p>Bits [6:5]=00</p> <p>One bit of data at a time from parallel bytes in each of the 4 memory planes is transferred to the palette via the 4 serial output bits, with 1 of each of the serial output bits corresponding to a memory plane. This provides a 4-bit value on each transfer for 1 pixel, making possible a choice of 1 of 16 colors per pixel.</p> <p>Serial</p> <table border="0"> <tr> <td>Out</td> <td>1st Xfer</td> <td>2nd Xfer</td> <td>3rd Xfer</td> <td>4th Xfer</td> <td>5th Xfer</td> <td>6th Xfer</td> <td>7th Xfer</td> <td>8th Xfer</td> </tr> <tr> <td>Bit 3</td> <td>plane3 bit7</td> <td>plane3 bit6</td> <td>plane3 bit5</td> <td>plane3 bit4</td> <td>plane3 bit3</td> <td>plane3 bit2</td> <td>plane3 bit1</td> <td>plane3 bit0</td> </tr> <tr> <td>Bit 2</td> <td>plane2 bit7</td> <td>plane2 bit6</td> <td>plane2 bit5</td> <td>plane2 bit4</td> <td>plane2 bit3</td> <td>plane2 bit2</td> <td>plane2 bit1</td> <td>plane2 bit0</td> </tr> <tr> <td>Bit 1</td> <td>plane1 bit7</td> <td>plane1 bit6</td> <td>plane1 bit5</td> <td>plane1 bit4</td> <td>plane1 bit3</td> <td>plane1 bit2</td> <td>plane1 bit1</td> <td>plane1 bit0</td> </tr> <tr> <td>Bit 0</td> <td>plane0 bit7</td> <td>plane0 bit6</td> <td>plane0 bit5</td> <td>plane0 bit4</td> <td>plane0 bit3</td> <td>plane0 bit2</td> <td>plane0 bit1</td> <td>plane0 bit0</td> </tr> </table> <p>Bits [6:5]=01</p> <p>Two bits of data at a time from parallel bytes in each of the 4 memory planes are transferred to the palette in a pattern that alternates per byte between memory planes 0 and 2, and memory planes 1 and 3. First the even-numbered and odd-numbered bits of a byte in memory plane 0 are transferred via serial output bits 0 and 1, respectively, while the even-numbered and odd-numbered bits of a byte in memory plane 2 are transferred via serial output bits 2 and 3. Next, the even-numbered and odd-numbered bits of a byte in memory plane 1 are transferred via serial output bits 0 and 1, respectively, while the even-numbered and odd-numbered bits of memory plane 3 are transferred via serial out bits 1 and 3. This provides a pair of 2-bit values (one 2-bit value for each of 2 pixels) on each transfer, making possible a choice of 1 of 4 colors per pixel.</p> <p>Serial</p> <table border="0"> <tr> <td>Out</td> <td>1st Xfer</td> <td>2nd Xfer</td> <td>3rd Xfer</td> <td>4th Xfer</td> <td>5th Xfer</td> <td>6th Xfer</td> <td>7th Xfer</td> <td>8th Xfer</td> </tr> <tr> <td>Bit 3</td> <td>plane2 bit7</td> <td>plane2 bit5</td> <td>plane2 bit3</td> <td>plane2 bit1</td> <td>plane3 bit7</td> <td>plane3 bit5</td> <td>plane3 bit3</td> <td>plane3 bit1</td> </tr> <tr> <td>Bit 2</td> <td>plane2 bit6</td> <td>plane2 bit4</td> <td>plane2 bit2</td> <td>plane2 bit0</td> <td>plane3 bit6</td> <td>plane3 bit4</td> <td>plane3 bit2</td> <td>plane3 bit0</td> </tr> <tr> <td>Bit 1</td> <td>plane0 bit7</td> <td>plane0 bit5</td> <td>plane0 bit3</td> <td>plane0 bit1</td> <td>plane1 bit7</td> <td>plane1 bit5</td> <td>plane1 bit3</td> <td>plane1 bit1</td> </tr> </table>	Out	1st Xfer	2nd Xfer	3rd Xfer	4th Xfer	5th Xfer	6th Xfer	7th Xfer	8th Xfer	Bit 3	plane3 bit7	plane3 bit6	plane3 bit5	plane3 bit4	plane3 bit3	plane3 bit2	plane3 bit1	plane3 bit0	Bit 2	plane2 bit7	plane2 bit6	plane2 bit5	plane2 bit4	plane2 bit3	plane2 bit2	plane2 bit1	plane2 bit0	Bit 1	plane1 bit7	plane1 bit6	plane1 bit5	plane1 bit4	plane1 bit3	plane1 bit2	plane1 bit1	plane1 bit0	Bit 0	plane0 bit7	plane0 bit6	plane0 bit5	plane0 bit4	plane0 bit3	plane0 bit2	plane0 bit1	plane0 bit0	Out	1st Xfer	2nd Xfer	3rd Xfer	4th Xfer	5th Xfer	6th Xfer	7th Xfer	8th Xfer	Bit 3	plane2 bit7	plane2 bit5	plane2 bit3	plane2 bit1	plane3 bit7	plane3 bit5	plane3 bit3	plane3 bit1	Bit 2	plane2 bit6	plane2 bit4	plane2 bit2	plane2 bit0	plane3 bit6	plane3 bit4	plane3 bit2	plane3 bit0	Bit 1	plane0 bit7	plane0 bit5	plane0 bit3	plane0 bit1	plane1 bit7	plane1 bit5	plane1 bit3	plane1 bit1
Out	1st Xfer	2nd Xfer	3rd Xfer	4th Xfer	5th Xfer	6th Xfer	7th Xfer	8th Xfer																																																																										
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Bit 2	plane2 bit6	plane2 bit4	plane2 bit2	plane2 bit0	plane3 bit6	plane3 bit4	plane3 bit2	plane3 bit0																																																																										
Bit 1	plane0 bit7	plane0 bit5	plane0 bit3	plane0 bit1	plane1 bit7	plane1 bit5	plane1 bit3	plane1 bit1																																																																										



Bit	Description																																													
	<p>Bit 0 plane0 bit6 plane0 bit4 plane0 bit2 plane0 bit0 plane1 bit6 plane1 bit4 plane1 bit2 plane1 bit0</p> <p>This alternating pattern is meant to accommodate the use of the Odd/Even mode of organizing the 4 memory planes, which is used by standard VGA modes 2h and 3h.</p> <p>Bits [6:5]=1x</p> <p>Four bits of data at a time from parallel bytes in each of the 4 memory planes are transferred to the palette in a pattern that iterates per byte through memory planes 0 through 3. First the 4 most significant bits of a byte in memory plane 0 are transferred via the 4 serial output bits, followed by the 4 least significant bits of the same byte. Next, the same transfers occur from the parallel byte in memory planes 1, 2 and lastly, 3. Each transfer provides either the upper or lower half of an 8 bit value for the color for each pixel, making possible a choice of 1 of 256 colors per pixel. This is the setting used in mode x13.</p> <p>Serial</p> <table border="0" data-bbox="321 693 1427 840"> <tr> <td>Out</td> <td>1st Xfer</td> <td>2nd Xfer</td> <td>3rd Xfer</td> <td>4th Xfer</td> <td>5th Xfer</td> <td>6th Xfer</td> <td>7th Xfer</td> <td>8th Xfer</td> </tr> <tr> <td>Bit 3</td> <td>plane0 bit7</td> <td>plane0 bit3</td> <td>plane1 bit7</td> <td>plane1 bit3</td> <td>plane2 bit7</td> <td>plane2 bit3</td> <td>plane3 bit7</td> <td>plane3 b3it</td> </tr> <tr> <td>Bit 2</td> <td>plane0 bit6</td> <td>plane0 bit2</td> <td>plane1 bit6</td> <td>plane1 bit2</td> <td>plane2 bit6</td> <td>plane2 bit2</td> <td>plane3 bit6</td> <td>plane3 bit2</td> </tr> <tr> <td>Bit 1</td> <td>plane0 bit5</td> <td>plane0 bit1</td> <td>plane1 bit5</td> <td>plane1 bit1</td> <td>plane2 bit5</td> <td>plane2 bit1</td> <td>plane3 bit5</td> <td>plane3 bit1</td> </tr> <tr> <td>Bit 0</td> <td>plane0 bit4</td> <td>plane0 bit0</td> <td>plane1 bit4</td> <td>plane1 bit0</td> <td>plane2 bit4</td> <td>plane2 bit0</td> <td>plane3 bit4</td> <td>plane3 bit0</td> </tr> </table> <p>This pattern is meant to accommodate mode 13h, a standard VGA 256-color graphics mode.</p>	Out	1st Xfer	2nd Xfer	3rd Xfer	4th Xfer	5th Xfer	6th Xfer	7th Xfer	8th Xfer	Bit 3	plane0 bit7	plane0 bit3	plane1 bit7	plane1 bit3	plane2 bit7	plane2 bit3	plane3 bit7	plane3 b3it	Bit 2	plane0 bit6	plane0 bit2	plane1 bit6	plane1 bit2	plane2 bit6	plane2 bit2	plane3 bit6	plane3 bit2	Bit 1	plane0 bit5	plane0 bit1	plane1 bit5	plane1 bit1	plane2 bit5	plane2 bit1	plane3 bit5	plane3 bit1	Bit 0	plane0 bit4	plane0 bit0	plane1 bit4	plane1 bit0	plane2 bit4	plane2 bit0	plane3 bit4	plane3 bit0
Out	1st Xfer	2nd Xfer	3rd Xfer	4th Xfer	5th Xfer	6th Xfer	7th Xfer	8th Xfer																																						
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Bit 2	plane0 bit6	plane0 bit2	plane1 bit6	plane1 bit2	plane2 bit6	plane2 bit2	plane3 bit6	plane3 bit2																																						
Bit 1	plane0 bit5	plane0 bit1	plane1 bit5	plane1 bit1	plane2 bit5	plane2 bit1	plane3 bit5	plane3 bit1																																						
Bit 0	plane0 bit4	plane0 bit0	plane1 bit4	plane1 bit0	plane2 bit4	plane2 bit0	plane3 bit4	plane3 bit0																																						
4	<p>Odd/Even Mode.</p> <p>0 = Addresses sequentially access data within a bit map, and the choice of which map is accessed is made according to the value of the Plane Mask Register (SR02).</p> <p>1 = The frame buffer is mapped in such a way that the function of address bit 0 is such that even addresses select memory planes 0 and 2 and odd addresses select memory planes 1 and 3.</p> <p>Note:This works in a way that is the inverse of (and is normally set to be the opposite of) bit 2 of the Memory Mode Register (SR02).</p>																																													
3	<p>Read Mode.</p> <p>0 = During a CPU read from the frame buffer, the value returned to the CPU is data from the memory plane selected by bits 1 and 0 of the Read Plane Select Register (GR04).</p> <p>1 = During a CPU read from the frame buffer, all 8 bits of the byte in each of the 4 memory planes corresponding to the address from which a CPU read access is being performed are compared to the corresponding bits in this register (if the corresponding bit in the Color Don't Care Register (GR07) is set to 1). The value that the CPU receives from the read access is an 8-bit value that shows the result of this comparison. A value of 1 in a given bit position indicates that all of the corresponding bits in the bytes across all 4 of the memory planes that were included in the comparison had the same value as their memory plane's respective bits in this register.</p>																																													
2	<p>Reserved. Read as 0.</p>																																													
1:0	<p>Write Mode.</p> <p>00 = Write Mode 0 - During a CPU write to the frame buffer, the addressed byte in each of the 4 memory planes is written with the CPU write data after it has been rotated by the number of counts specified in the Data Rotate Register (GR03). If, however, the bit(s) in the Enable Set/Reset Register (GR01) corresponding to one or more of the memory planes is set to 1, then those memory planes will be written to with the data stored in the corresponding bits in the Set/Reset Register (GR00).</p>																																													



Bit	Description
01 =	Write Mode 1 - During a CPU write to the frame buffer, the addressed byte in each of the 4 memory planes is written to with the data stored in the memory read latches. (The memory read latches stores an unaltered copy of the data last read from any location in the frame buffer.)
10 =	Write Mode 2 - During a CPU write to the frame buffer, the least significant 4 data bits of the CPU write data is treated as the color value for the pixels in the addressed byte in all 4 memory planes. The 8 bits of the Bit Mask Register (GR08) are used to selectively enable or disable the ability to write to the corresponding bit in each of the 4 memory planes that correspond to a given pixel. A setting of 0 in a bit in the Bit Mask Register at a given bit position causes the bits in the corresponding bit positions in the addressed byte in all 4 memory planes to be written with value of their counterparts in the memory read latches. A setting of 1 in a Bit Mask Register at a given bit position causes the bits in the corresponding bit positions in the addressed byte in all 4 memory planes to be written with the 4 bits taken from the CPU write data to thereby cause the pixel corresponding to these bits to be set to the color value.
11 =	Write Mode 3 - During a CPU write to the frame buffer, the CPU write data is logically ANDed with the contents of the Bit Mask Register (GR08). The result of this ANDing is treated as the bit mask used in writing the contents of the Set/Reset Register (GR00) are written to addressed byte in all 4 memory planes.

1.3.8 GR06 - Miscellaneous Register

I/O (and Memory Offset) Address:3CFh (Index=06h)

Default: 0Uh (U=Undefined)

Attributes:Read/Write

7 43 2 1 0
Reserved (0000)Memory Map ModeChain Odd/EvenGraphics / Text Mode

Bit	Description
7:4	Reserved. Read as 0s.
3:2	<p>Memory Map Mode. These 2 bits control the mapping of the VGA address range for frame buffer into the CPU address space as follows:</p> <p>00 = A0000h - BFFFFh 01 = A0000h - AFFFFh 10 = B0000h - B7FFFh 11 = B8000h - BFFFFh</p> <p>Note:</p> <ul style="list-style-type: none"> This function is used in standard VGA modes, extended VGA modes (132 column text), and in non-VGA modes (hi-res). 132 column text modes are no longer supported. VGA aperture memory accesses are also controlled by the PCI configuration Memory Enable bit and MSR<1>. For accesses using GR10 and GR11 to paged VGA RAM or to device MMIO registers, set these bits to



Bit	Description
	01 to select the (A0000-AFFFF) range. <ul style="list-style-type: none"> The CPU must map this memory as uncacheable (UC).
1	Chain Odd/Even. This bit provides the ability to alter the interpretation of address bit A0, so that it may be used in selecting between the odd-numbered memory planes (planes 1 and 3) and the even-numbered memory planes (planes 0 and 2). 0 = A0 functions normally. 1 = A0 is switched with a high order address bit, in terms of how it is used in address decoding. The result is that A0 is used to determine which memory plane is being accessed (A0=0 for planes 0 and 2 and A0=1 for planes 1 and 3).
0	Graphics/Text Mode. This is one of two bits that are used to determine if the VGA is operating in text or graphics modes. The other bit is in AR10[0], these two bits need to be programmed in a consistent manner to achieve the proper results. 0 = Text mode. 1 = Graphics mode.

1.3.9 GR07 - Color Don't Care Register

I/O (and Memory Offset) Address:3CFh (Index=07h)

Default: 0Uh (U=Undefined)

Attributes:Read/Write

7	4	3	2	1	0
Reserved (0000)	Ignore	Ignore	Ignore	Ignore	Ignore
	Color Plane 3	Color Plane 2	Color Plane 1	Color Plane 0	

Bit	Description
7:4	Reserved. Read as 0.
3:0	Ignore Color Plane [3:0]. Note that these bits have effect only when bit 3 of the Graphics Mode Register (GR05) is set to 1 to select read mode 1. 0 = The corresponding bit in the Color Compare Register (GR02) will not be included in color comparisons. 1 = The corresponding bit in the Color Compare Register (GR02) is used in color comparisons.



1.3.10 GR08 - Bit Mask Register

I/O (and Memory Offset) Address:3CFh (Index=08h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	<p>Bit Mask.</p> <p>0 = The corresponding bit in each of the 4 memory planes is written to with the corresponding bit in the memory read latches.</p> <p>1 = Manipulation of the corresponding bit in each of the 4 memory planes via other mechanisms is enabled.</p> <p>Notes:</p> <ul style="list-style-type: none">• This bit mask applies to any writes to the addressed byte of any or all of the 4 memory planes, simultaneously.• This bit mask is applicable to any data written into the frame buffer by the CPU, including data that is also subject to rotation, logical functions (AND, OR, XOR), and Set/Reset. To perform a proper read-modify-write cycle into frame buffer, each byte must first be read from the frame buffer by the CPU (and this will cause it to be stored in the memory read latches), this Bit Mask Register must be set, and the new data then written into the frame buffer by the CPU.

1.3.11 GR10 - Address Mapping

I/O (avoid MMIO access) Address:3CFh (Index=10h)

Default:00h

Attributes:R/W

This register should only be accessed using I/O operations and never be accessed through the A/B segment addressing map, I/O space register map, or direct MMIO operations.

Bit	Description
7:4	<p>Page Select Extension - Unused</p> <p>These bits form the upper bits of a 12-bit page selection value. When combined with the GR11 <7:0> bits they define the offset into stolen memory to the 64KB page that is accessible via the VGA Memory paging mechanism.</p> <p>These bits are ignored.</p>
3	<p>Reserved</p>
2:1	<p>Paging Map Target.</p> <p>When paging is enabled, these bits determine the target for data cycle accesses through the VGA memory aperture.</p> <p>VGA graphics memory starts from the base of graphics data stolen memory defined in the PCI configuration BDSM register.</p> <p>VGA display uses the first four 64KB pages of VGA graphics memory.</p>



Bit	Description
	00 = VGA Graphics Memory 01 = Reserved 10 = Reserved 11 = Reserved
0	Page Mapping Enable. This mode allows the mapping of the VGA memory address space. Some Notes on Paging. Once this is enabled, no VGA memory address swizzel will be performed, addresses are directly mapped to memory. A single paging register is used to map the 64KB [A0000:AFFFF] window. An internal address is generated using GR11 as the address lines extension to the lower address lines of the access A[15:2]. When mapping is enabled, the B0000:BFFFF area must be disabled using GR06<3:2>=01. The use of addresses in the A0000-BFFFF range require that both the graphics device PCI configuration memory enable and MSR<1> be enabled. 0 = Disable (default) 1 = Enable

1.3.12 GR11 - Page Selector

I/O Address (avoid MMIO access):3CFh (Index=11h)

Default: 00h

Attributes:R/W

Bit	Description
7	Reserved
6:0	Page Select. When concatenated with the GR10<7:4> bits, selects a 64KB window within target area when Page Mapping is enabled (GR10[0]=1). This requires that the graphics device PCI configuration space memory enable, the GR06<3:2> bits to be 01 (select A0000-AFFFF only), and the MSR<1:1> bit to be set. This register provides the Address[22:16] bits for the access. VGA paging of frame buffer memory is for non-VGA packed modes only and should not be enabled when using basic VGA modes. This register should only be accessed using I/O operations.



Bit	Description
	<p>will cause the VGA display data to become all 00 index values. For the default palette, this will cause a black screen. The video timing signals continue. Another control bit will turn video off and stop the data fetches.</p> <p>0 = Disable. Attribute controller color registers (AR[00:0F]) can be accessed by the CPU.</p> <p>1 = Enable. Attribute controller color registers (AR[00:0F]) are inaccessible by the CPU.</p>
4:0	<p>Attribute Controller Register Index. These five bits are used to select any one of the attribute controller registers (AR[00:14]), to be accessed.</p> <p>Note:AR12 is referred to in the VGA standard as the Color Plane Enable Register. The words “plane,” “color plane,” “display memory plane,” and “memory map” have been all been used in literature on the VGA standard to describe the four separate regions in the frame buffer where the pixel color or attribute information is split up and stored in standard VGA planar modes. This use of multiple terms for the same subject was deemed to be confusing, therefore, AR12 is called the Memory Plane Enable Register. Attribute Controller Register Index.</p>

1.4.2 AR[00:0F] - Palette Registers [0:F]

I/O (and Memory Offset) Address:Read at 3C1h and Write at 3C0h; (index=00h-0Fh)

Default:00UU UUUUb (U=Undefined)

Attributes:Read/Write

7 65 0

ReservedPalette Bits P[5:0]

Bit	Description
7:6	Reserved. Read as 0.
5:0	<p>Palette Bits P[5:0]. In each of these 16 registers, these are the lower 6 of 8 bits that are used to map either text attributes or pixel color input values (for modes that use 16 colors) to the 256 possible colors available to be selected in the palette.</p> <p>Note:Bits 3 and 2 of the Color Select Register (AR14) supply bits P7 and P6 for the values contained in all 16 of these registers. Bits 1 and 0 of the Color Select Register (AR14) can also replace bits P5 and P4 for the values contained in all 16 of these registers, if bit 7 of the Mode Control Register (AR10) is set to 1.</p>



1.4.3 AR10 - Mode Control Register

I/O (and Memory Offset) Address:	Read at 3C1h and Write at 3C0h; (index=10h)
Default:	UUh (U=Undefined)
Attributes:	Read/Write

7	6	5	4	3	2	1	0
Palette Bits P5, P4 Select	Pixel Width/ Clock Select	Pixel Panning Compat	Reserved (0)	Enable Blink/ Select Bkgnd Int	Enable Line Graphics Char Code	Select Display Type	Graphics/ Alpha Mode

Bit	Description
7	<p>Palette Bits P5, P4 Select.</p> <p>0 = P5 and P4 for each of the 16 selected colors (for modes that use 16 colors) are individually provided by bits 5 and 4 of their corresponding Palette Registers (AR[00:0F]).</p> <p>1 = P5 and P4 for all 16 of the selected colors (for modes that use 16 colors) are provided by bits 1 and 0 of Color Select Register (AR14).</p>
6	<p>Pixel Width/Clock Select.</p> <p>0 = Six bits of video data (translated from 4 bits via the palette) are output every dot clock.</p> <p>1 = Two sets of 4 bits of data are assembled to generate 8 bits of video data which is output every other dot clock, and the Palette Registers (AR[00:0F]) are bypassed.</p> <p>Note: This bit is set to 0 for all of the standard VGA modes, except mode 13h.</p>
5	<p>Pixel Panning Compatibility.</p> <p>0 = Scroll both the upper and lower screen regions horizontally as specified in the Pixel Panning Register (AR13).</p> <p>1 = Scroll only the upper screen region horizontally as specified in the Pixel Panning Register (AR13).</p> <p>Note: This bit has application only when split-screen mode is being used, where the display area is divided into distinct upper and lower regions which function somewhat like separate displays.</p>
4	<p>Reserved. Read as 0.</p>
3	<p>Enable Blinking/Select Background Intensity.</p> <p>0 = Disables blinking in graphics modes, and for text modes, sets bit 7 of the character attribute bytes to control background intensity, instead of blinking.</p> <p>1 = Enables blinking in graphics modes and for text modes, sets bit 7 of the character attribute bytes to control blinking, instead of background intensity.</p> <p>Note: The blinking rate is derived by dividing the VSYNC signal. The Blink Rate Control field of the VGA control register defines the blinking rate.</p>
2	<p>Enable Line Graphics Character Code.</p> <p>0 = Every 9th pixel of a horizontal line (i.e., the last pixel of each horizontal line of each 9-pixel wide character box) is assigned the same attributes as the background of the character of which the given pixel is a part.</p>



Bit	Description
	<p>1 = Every 9th pixel of a horizontal line (i.e., the last pixel of each horizontal line of each 9-pixel wide character box) is assigned the same attributes as the 8th pixel if the character of which the given pixel is a part. This setting is intended to accommodate the line-drawing characters of the PC's extended ASCII character set -- characters with an extended ASCII code in the range of B0h to DFh.</p> <p>Note: In some literature describing the VGA standard, the range of extended ASCII codes that are said to include the line-drawing characters is mistakenly specified as C0h to DFh, rather than the correct range of B0h to DFh.</p>
1	<p>Select Display Type.</p> <p>0 = Attribute bytes in text modes are interpreted as they would be for a color display.</p> <p>1 = Attribute bytes in text modes are interpreted as they would be for a monochrome display.</p>
0	<p>Graphics/Alphanumeric Mode. This bit (along with GR06[0]) select either graphics mode or text mode. These two bits must be programmed in a consistent manner to achieve the desired results.</p> <p>0 = Alphanumeric (text) mode.</p> <p>1 = Graphics mode.</p>

1.4.4 AR12 - Memory Plane Enable Register

I/O (and Memory Offset) Address: Read at 3C1h and Write at 3C0h; (index=12h)

Default: 00UU UUUUb (U=Undefined)

Attributes: Read/Write

7 65 4 3 2 1 0
 Reserved (00) Video Status Mux Enable Plane 3 Enable Plane 2 Enable Plane 1 Enable Plane 0

Bit	Description															
7:6	Reserved. Read as 0.															
5:4	<p>Video Status Mux. These 2 bits are used to select 2 of the 8 possible palette bits (P7-P0) to be made available to be read via bits 5 and 4 of the Input Status Register 1 (ST01). The table below shows the possible choices.</p> <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit [5:4]</th> <th>ST01 Bit 5</th> <th>ST01 Bit 4</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>P2 (default)</td> <td>P0 (default)</td> </tr> <tr> <td>01</td> <td>P5</td> <td>P4</td> </tr> <tr> <td>10</td> <td>P3</td> <td>P1</td> </tr> <tr> <td>11</td> <td>P7</td> <td>P6</td> </tr> </tbody> </table> <p>These bits are typically unused by current software; they are provided for EGA compatibility.</p>	Bit [5:4]	ST01 Bit 5	ST01 Bit 4	00	P2 (default)	P0 (default)	01	P5	P4	10	P3	P1	11	P7	P6
Bit [5:4]	ST01 Bit 5	ST01 Bit 4														
00	P2 (default)	P0 (default)														
01	P5	P4														
10	P3	P1														
11	P7	P6														
3:0	<p>Enable Plane [3:0]. These 4 bits individually enable the use of each of the 4 memory planes in providing 1 of the 4 bits used in video output to select 1 of 16 possible colors from the palette to be displayed.</p> <p>0 = Disable the use of the corresponding memory plane in video output to select colors, forcing the bit</p>															



Bit	Description
1 =	<p>that the corresponding memory plane would have provided to a value of 0. Enable the use of the corresponding memory plane in video output to select colors.</p> <p>Note: AR12 is referred to in the VGA standard as the Color Plane Enable Register. The words “plane,” “color plane,” “display memory plane,” and “memory map” have been all been used in literature on the VGA standard to describe the 4 separate regions in the frame buffer that are amongst which pixel color or attributes information is split up and stored in standard VGA planar modes. This use of multiple terms for the same subject was considered confusing; therefore, AR12 is called the Memory Plane Enable Register.</p>

1.4.5 AR13 - Horizontal Pixel Panning Register

I/O (and Memory Offset) Address:Read at 3C1h and Write at 3C0h; (index=13h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7 43 0
Reserved (0000)Horizontal Pixel Shift

Bit	Description																																																							
7:4	Reserved.																																																							
3:0	<p>Horizontal Pixel Shift 3-0. This field holds a 4-bit value that selects the number of pixels by which the image is shifted horizontally to the left. This function is available in both text and graphics modes and allows for pixel panning.</p> <p>In text modes with a 9-pixel wide character box, the image can be shifted up to 9 pixels to the left. In text modes with an 8-pixel wide character box, and in graphics modes other than those with 256 colors, the image can be shifted up to 8 pixels to the left. A pseudo 9-bit mode is when the 9-dot character is selected but overridden by the VGA control bit.</p> <p>In standard VGA mode 13h (where bit 6 of the Mode Control Register, AR10, is set to 1 to support 256 colors), bit 0 of this register must remain set to 0, and the image may be shifted up to only 4 pixels to the left. In this mode, the number of pixels by which the image is shifted can be further controlled using bits 6 and 5 of the Preset Row Scan Register (CR08).</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="5" style="text-align: center; color: blue;">Number of Pixels Shifted</th> </tr> <tr> <th style="text-align: left; color: blue;">Bits [3:0]</th> <th style="text-align: center; color: blue;">9-dot</th> <th style="text-align: center; color: blue;">Pseudo 9-dot</th> <th style="text-align: center; color: blue;">8-dot</th> <th style="text-align: center; color: blue;">256-Color</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">2</td><td style="text-align: center;">2</td><td style="text-align: center;">1</td><td style="text-align: center;">Undefined</td></tr> <tr><td style="text-align: center;">2</td><td style="text-align: center;">3</td><td style="text-align: center;">3</td><td style="text-align: center;">2</td><td style="text-align: center;">1</td></tr> <tr><td style="text-align: center;">3</td><td style="text-align: center;">4</td><td style="text-align: center;">4</td><td style="text-align: center;">3</td><td style="text-align: center;">Undefined</td></tr> <tr><td style="text-align: center;">4</td><td style="text-align: center;">5</td><td style="text-align: center;">5</td><td style="text-align: center;">4</td><td style="text-align: center;">2</td></tr> <tr><td style="text-align: center;">5</td><td style="text-align: center;">6</td><td style="text-align: center;">6</td><td style="text-align: center;">5</td><td style="text-align: center;">Undefined</td></tr> <tr><td style="text-align: center;">6</td><td style="text-align: center;">7</td><td style="text-align: center;">7</td><td style="text-align: center;">6</td><td style="text-align: center;">3</td></tr> <tr><td style="text-align: center;">7</td><td style="text-align: center;">8</td><td style="text-align: center;">7</td><td style="text-align: center;">7</td><td style="text-align: center;">Undefined</td></tr> <tr><td style="text-align: center;">8</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">Undefined</td><td style="text-align: center;">Undefined</td></tr> </tbody> </table>	Number of Pixels Shifted					Bits [3:0]	9-dot	Pseudo 9-dot	8-dot	256-Color	0	1	1	0	0	1	2	2	1	Undefined	2	3	3	2	1	3	4	4	3	Undefined	4	5	5	4	2	5	6	6	5	Undefined	6	7	7	6	3	7	8	7	7	Undefined	8	0	0	Undefined	Undefined
Number of Pixels Shifted																																																								
Bits [3:0]	9-dot	Pseudo 9-dot	8-dot	256-Color																																																				
0	1	1	0	0																																																				
1	2	2	1	Undefined																																																				
2	3	3	2	1																																																				
3	4	4	3	Undefined																																																				
4	5	5	4	2																																																				
5	6	6	5	Undefined																																																				
6	7	7	6	3																																																				
7	8	7	7	Undefined																																																				
8	0	0	Undefined	Undefined																																																				



1.4.6 AR14 - Color Select Register

I/O (and Memory Offset) Address:Read at 3C1h and Write at 3C0h; (index=14h)

Default:0Uh (U=Undefined)

Attributes:Read/Write

7		4 3 2 1 0
	Reserved (0000)	P7 P6 Alt P5 Alt P4

Bit	Description
7:4	Reserved.
3:2	Palette Bits P[7:6]. These are the 2 upper-most of the 8 bits that are used to map either text attributes or pixel color input values (for modes that use 16 colors) to the 256 possible colors contained in the palette. These 2 bits are common to all 16 sets of bits P5 through P0 that are individually supplied by Palette Registers 0-F (AR[00:0F]).
1:0	Alternate Palette Bits P[5:4]. These 2 bits can be used as an alternate version of palette bits P5 and P4. Unlike the P5 and P4 bits that are individually supplied by Palette Registers 0-F (AR[00:0F]), these 2 alternate palette bits are common to all 16 of Palette Registers. Bit 7 of the Mode Control Register (AR10) is used to select between the use of either the P5 and P4 bits that are individually supplied by the 16 Palette Registers or these 2 alternate palette bits.

1.5 VGA Color Palette Registers

In devices that have multiple display pipes, there is one palette for each display pipe. These palettes are the same for VGA modes and non-VGA modes. Accesses through VGA register methods can optionally read or write from either one.

For each palette, the color data stored in these 256 color data positions can be accessed only through a complex sub-addressing scheme, using a data register and two index registers. The Palette Data Register at I/O address 3C9h (or memory address offset 3C1h) is the data port. The Palette Read Index Register at I/O address 3C7h (or memory address offset 3C7h) and the Palette Write Index Register at I/O address 3C8h (or memory address offset 3C8h) are the two index registers. The Palette Read Index Register is the index register that is used to choose the color data position that is to be read from via the data port, while the Palette Write Index Register is the index register that is used to choose the color data position that is to be written to through the same data port. This arrangement allows the same data port to be used for reading from and writing to two different color data positions. Reading and writing the color data at a color data position involves three successive reads or writes since the color data stored at each color data position consists of three bytes.

To read a palette color data position, the index of the desired color data position must first be written to the Palette Read Index Register. Then all three bytes of data in a given color data position may be read at the Palette Data Register. The first byte read from the Palette Data Register retrieves the 8-bit value specifying the intensity of the red color component. The second and third bytes read are the corresponding 8-bit values for the green and blue color components respectively. After completing the third read operation, the Palette Read Index Register is automatically incremented so that the data of the next color data position becomes accessible for being read. This allows the contents of all of the 256



color data positions of the palette to be read in sequence. This is done by specifying only the index of the 0th color data position in the Palette Read Index Register, and then simply performing 768 successive reads from the Palette Data Register.

Writing a color data position, entails a very similar procedure. The index of the desired color data position must first be written to the Palette Write Index Register. Then all three bytes of data to specify a given color may be written to the Palette Data Register. The first byte written to the Palette Data Register specifies the intensity of the red color component, the second byte specifies the intensity for the green color component, and the third byte specifies the same for the blue color component. One important detail is that all three of these bytes must be written before the hardware will actually update these three values in the given color data position. When all three bytes have been written, the Palette Write Index Register is automatically incremented so that the data of the next color data position becomes accessible for being written. This allows the contents of all of the 256 color data positions of the palette to be written in sequence. This is done by specifying only the index of the 0th color data position in the Palette Write Index Register, and then simply performing 768 successive writes to the Palette Data Register.

1.5.1 DACMASK - Pixel Data Mask Register

I/O (and Memory Offset) Address:3C6h

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	<p>Pixel Data Mask. In indexed-color mode, the 8 bits of this register are logically ANDed with the 8 bits of pixel data received from the frame buffer for each pixel. The result of this ANDing process becomes the actual index used to select color data positions within the palette. This has the effect of limiting the choice of color data positions that may be specified by the incoming 8-bit data.</p> <p>0 = Corresponding bit in the resulting 8-bit index being forced to 0.</p> <p>1 = Allows the corresponding bit in the resulting index to reflect the actual value of the corresponding bit in the incoming 8-bit pixel data.</p>



1.5.2 DACSTATE – DAC State Register

I/O (and Memory Offset) Address:3C7h

Default:00h

Attributes:Read Only

7 21 0
Reserved (000000)DAC State

Bit	Description
7:2	Reserved. Read as 0.
1:0	DACState. This field indicates which of the two index registers was most recently written. Bits [1:0] Index Register Indicated 00 = Palette Write Index Register at I/O Address 3C7h (default) 01 = Reserved 10 = Reserved 11 = Palette Read Index Register at I/O Address 3C8h

1.5.3 DACRX - Palette Read Index Register

I/O (and Memory Offset) Address:3C7h

Default:00h

Attributes:Write Only

Bit	Description
7:0	Palette Read Index. The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being read from via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been read. A write to this register will abort a uncompleted palette write sequence. This register allows access to the palette even when running non-VGA display modes.



1.5.4 DACWX - Palette Write Index Register

I/O (and Memory Offset) Address:3C8h

Default:00h

Attributes:Write Only

Bit	Description
7:0	Palette Write Index. The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being written via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been written. This register allows access to the palette even when running non-VGA display modes.

1.5.5 DACDATA - Palette Data Register

I/O (and Memory Offset) Address:3C9h

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Palette Data. This byte-wide data port provides read or write access to the three bytes of data of each color data position selected using the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX). The three bytes in each color data position are read or written in three successive read or write operations. The first byte read or written specifies the intensity of the red component of the color specified in the selected color data position. The second byte is for the green component, and the third byte is for the blue component. When writing data to a color data position, all three bytes must be written before the hardware will actually update the three bytes of the selected color data position. When reading or writing to a color data position, ensure that neither the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX) are written to before all three bytes are read or written. A write to either of these two registers causes the circuitry that automatically cycles through providing access to the bytes for red, green and blue components to be reset such that the byte for the red component is the one that will be accessed by the next read or write operation via this register. This register allows access to the palette even when running non-VGA display modes. Writes to the palette can cause sparkle if not done during inactive video periods. This sparkle is caused by an attempt to write and read the same address on the same cycle. Anti-sparkle circuits will substitute the previous pixel value for the read output.

1.6 CRT Controller Register

For native VGA modes, the CRT registers determine the display timing that is to be used. In centered VGA modes, these registers determine the size of the VGA image that is to be centered in the larger timing generator defined rectangle.

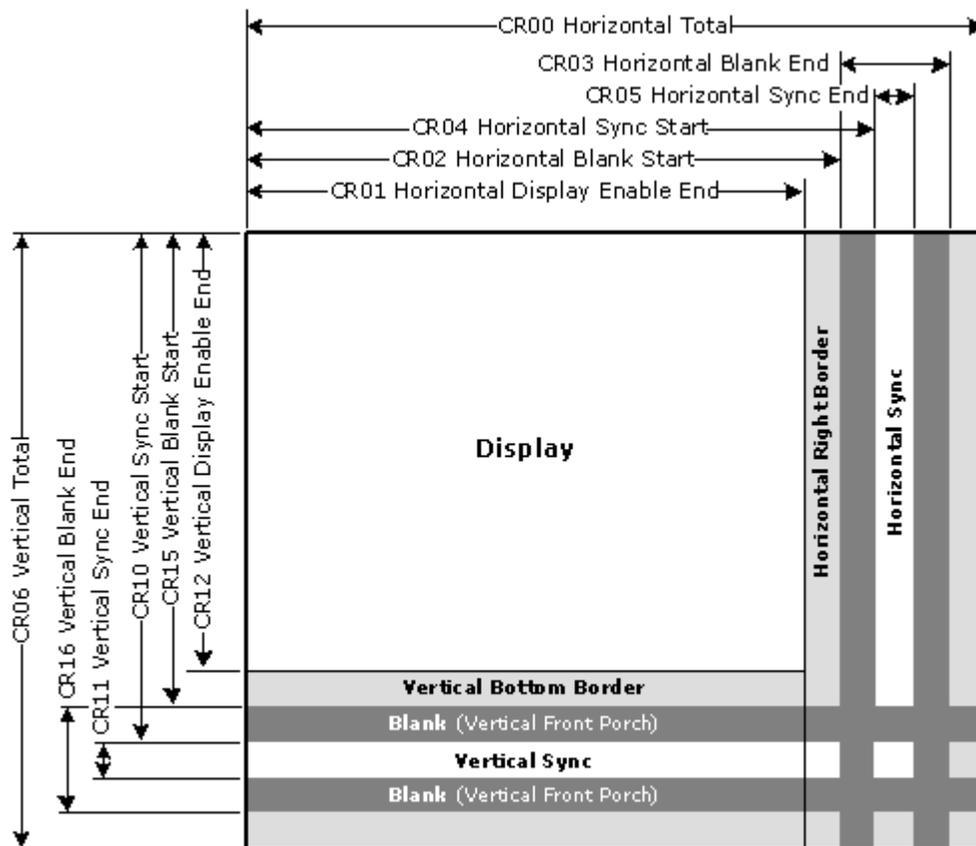
The CRT controller registers are accessed by writing the index of the desired register into the CRT Controller Index Register at I/O address 3B4h or 3D4h, depending on whether the graphics system is configured for MDA or CGA emulation. The desired register is then accessed through the data port for the CRT controller registers located at I/O address 3B5h or 3D5h, again depending upon the choice of MDA

or CGA emulation as per MSR[0]. For memory mapped accesses, the Index register is at 3B4h (MDA mode) or 3D3h (CGA mode) and the data port is accessed at 3B5h (MDA mode) or 3D5h (CGA mode).

Note:

1. **Group 0 Protection:** In the original VGA, CR[0:7] could be made write-protected by CR11[7]. In BIOS code, this write protection is set following each mode change. Other protection groups have no current use, and would not be used going forward by the BIOS or by drivers. They are the result of an industry fad some years ago to attempt to write protect other groups of registers; however, all such schemes were chip specific. Only the write protection (Group 0 Protection) is supported.

The following figure shows display fields and dimensions and the particular CRxx register that provides the control.



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1.6.1 CRX - CRT Controller Index Register

I/O (and Memory Offset) Address:3B4h/3D4h

Default:0Uh (U=Undefined)

Attributes:Read/Write

Bit	Description
7	Reserved. Read as 0.
6:0	CRT Controller Index. These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

1.6.2 CR00 - Horizontal Total Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=00h)

Default:00h

Attributes:Read/Write (Group 0 Protection)

Bit	Description
7:0	Horizontal Total. This register is used to specify the total length of each scan line. This encompasses both the part of the scan line that is within the active display area and the part that is outside of it. Programming this register to a zero has the effect of stopping the fetching of display data. This field should be programmed with a value equal to the total number of character clocks within the entire length of a scan line, minus 5.

1.6.3 CR01 - Horizontal Display Enable End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=01h)

Default:Undefined

Attributes:Read/Write (Group 0 Protection)

Bit	Description
7:0	Horizontal Display Enable End. This register is used to specify the end of the part of the scan line that is within the active display area relative to its beginning. In other words, this is the horizontal width of the active display area. This field should be programmed with a value equal to the number of character clocks that occur within the horizontal active display area, minus 1. Horizontal display enable will go active at the beginning of each line during vertical active area, it will go inactive based on the programming of this register or the programming of the horizontal total (CR00) register. When this register value is programmed to a number that is larger than the total number of characters on a line, display enable will be active for all but the last character of the horizontal display line.



1.6.4 CR02 - Horizontal Blanking Start Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=02h)

Default:Undefined

Attributes:Read/Write (Group 0 Protection)

Bit	Description
7:0	<p>Horizontal Blanking Start. This register is used to specify the beginning of the horizontal blanking period relative to the beginning of the active display area of a scan line. Horizontal blanking should always be set to start no sooner than after the end of horizontal active.</p> <p>This field should be programmed with a value equal to the number of character clocks that occur on a scan line from the beginning of the active display area to the beginning of the horizontal blanking.</p>

1.6.5 CR03 - Horizontal Blanking End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=03h)

Default:1UUU UUUUb (U=Undefined)

Attributes:Read/Write (Group 0 Protection)

7 6 54 0
ReservedDisplay Enable Skew ControlHorizontal Blanking End Bits 4:0

Bit	Description
7	<p>Reserved. Values written to this bit are ignored, and to maintain consistency with the VGA standard, a value of 1 is returned when this bit is read. At one time, this bit was used to enable access to certain light pen registers. At that time, setting this bit to 0 provided this access, but setting this bit to 1 was necessary for normal operation.</p>
6:5	<p>Display Enable Skew Control. Defines the degree to which the start and end of the active display area are delayed along the length of a scan line to compensate for internal pipeline delays. These 2 bits describe the delay in terms of a number character clocks.</p> <p>Bit [6:5] Amount of Delay</p> <p>00 = no delay</p> <p>01 = delayed by 1 character clock</p> <p>10 = delayed by 2 character clocks</p> <p>11 = delayed by 3 character clocks</p>
4:0	<p>Horizontal Blanking End Bits [4:0]. This field provides the 5 least significant bits of a 6-bit value that specifies the end of the blanking period relative to its beginning on a single scan line. Bit 7 of the Horizontal Sync End Register (CR05) supplies the most significant bit.</p> <p>This 6-bit value should be programmed to be equal to the least significant 6 bits of the result of adding the length of the blanking period in terms of character clocks to the value specified in the Horizontal Blanking Start Register (CR02). End of blanking should occur before horizontal total.</p>



1.6.6 CR04 - Horizontal Sync Start Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=04h)

Default:Undefined

Attributes:Read/Write (Group 0 Protection)

Bit	Description
7:0	<p>Horizontal Sync Start This register is used to specify the position of the beginning of the horizontal sync pulse relative to the start of the active display area on a scan line.</p> <p>This field should be set equal to the number of character clocks that occur from beginning of the active display area to the beginning of the horizontal sync pulse on a single scan line. Horizontal sync should always occur at least 2 clocks after the start of horizontal blank and 2 clocks before the end of horizontal blank. The actual start of sync will also be affected by both the horizontal sync skew register field and whether it is a text or graphics mode.</p>

1.6.7 CR05 - Horizontal Sync End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=05h)

Default:00h

Attributes:Read/Write (Group 0 Protection)

7 6 54 0
 Hor Blank End <5>Horizontal Sync DelayHorizontal Sync End

Bit	Description										
7	<p>Horizontal Blanking End Bit 5. This bit provides the most significant bit of a 6-bit value that specifies the end of the horizontal blanking period relative to its beginning. Bits [4:0] of Horizontal Blanking End Register (CR03) supplies the 5 least significant bits. See CR03[4:0] for further details.</p> <p>This 6-bit value should be set to the least significant 6 bits of the result of adding the length of the blanking period in terms of character clocks to the value specified in the Horizontal Blanking Start Register (CR02).</p>										
6:5	<p>Horizontal Sync Delay. This field defines the degree to which the start and end of the horizontal sync pulse are delayed to compensate for internal pipeline delays. This capability is supplied to implement VGA compatibility. These field describes the delay in terms of a number character clocks.</p> <table border="1"> <thead> <tr> <th>Bit [6:5]</th> <th>Amount of Delay</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>no delay</td> </tr> <tr> <td>01</td> <td>delayed by 1 character clock</td> </tr> <tr> <td>10</td> <td>delayed by 2 character clocks</td> </tr> <tr> <td>11</td> <td>delayed by 3 character clocks</td> </tr> </tbody> </table>	Bit [6:5]	Amount of Delay	00	no delay	01	delayed by 1 character clock	10	delayed by 2 character clocks	11	delayed by 3 character clocks
Bit [6:5]	Amount of Delay										
00	no delay										
01	delayed by 1 character clock										
10	delayed by 2 character clocks										
11	delayed by 3 character clocks										
4:0	<p>Horizontal Sync End. This field provides the 5 least significant bits of a 5-bit value that specifies the end of the horizontal sync pulse relative to its beginning. A value equal to the 5 least significant bits of the horizontal character counter value at which time the horizontal retrace signal becomes inactive (logical 0). Thus, this 5-bit value specifies the width of the horizontal sync pulse. To obtain a retrace signal of W, the following</p>										



Bit	Description
	algorithm is used: Value of Horizontal Sync start Register (CR04) + width of horizontal retrace signal in character clock units = 5 bit result to be programmed in this field

1.6.8 CR06 - Vertical Total Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=06h)

Default:00h

Attributes:Read/Write (Group 0 Protection)

Bit	Description
7:0	<p>Vertical Total Bits [7:0]. This field provides the 8 least significant bits of either a 10-bit or 12-bit value that specifies the total number of scan lines. This includes the scan lines both inside and outside of the active display area.</p> <p>In standard VGA modes, the vertical total is specified with a 10-bit value. The 8 least significant bits of this value are supplied by these 8 bits of this register, and the 2 most significant bits are supplied by bits 5 and 0 of the Overflow Register (CR07).</p>

1.6.9 CR07 - Overflow Register (Vertical)

I/O (and Memory Offset) Address:3B5h/3D5h (index=07h)

Default:UU0U UUU0b (U=Undefined)

Attributes:Read/Write (Group 0 Protection on bits [7:5, 3:0])

7	6	5	4	3	2	1	0
Vert Sync Start <9>	Vert Disp Enable <9>	Vert Total <9>	Line Cmp<8>	Vert Blank Start<8>	Vert Sync Start<8>	Vert Display Enable <8>	Vert Total <8>

Bit	Description
7	<p>Vertical Sync Start Bit 9. The vertical sync start is a 10-bit that specifies the beginning of the vertical sync pulse relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Sync Start Register (CR10), and the most and second-most significant bits are supplied by this bit and bit 2, respectively, of this register. This 10-bit value should be programmed to be equal to the number of scan lines from the beginning of the active display area to the start of the vertical sync pulse. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical sync pulse begins.</p>
6	<p>Vertical Display Enable End Bit 9. The vertical display enable end is a 10-bit that specifies the number of the last scan line within the active display area. In standard VGA modes, the vertical display enable end is specified with a 10-bit value. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Display Enable End Register (CR12), and the most and second-most significant bits are supplied by this bit and bit 1, respectively, of this register. This 10-bit value should be programmed to be equal to the number of the last scan line within in the active display area. Since the active display area always starts on the 0th scan line, this number should be equal to the total number of scan lines within the active display area, minus 1.</p>
5	<p>Vertical Total Bit 9. The vertical total is a 10-bit value that specifies the total number of scan lines. This includes the scan lines both inside and outside of the active display area. The 8 least significant bits of this</p>



Bit	Description
	<p>value are supplied by bits [7:0] of the Vertical Total Register (CR06), and the most and second-most significant bits are supplied by this bit and bit 0, respectively, of this register.</p> <p>This 10-bit value should be programmed equal to the total number of scan lines, minus 2.</p>
4	<p>Line Compare Bit 8. This bit provides the second most significant bit of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 6 of the Maximum Scan Line Register (CR09) supplies the most significant bit, and bits 7-0 of the Line Compare Register (CR18) supply the 8 least significant bits. Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part. When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display what data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display what data exists in the frame buffer starting at the first byte of the frame buffer.</p>
3	<p>Vertical Blanking Start Bit 8. The vertical blanking start is a 10-bit that specifies the beginning of the vertical blanking period relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Blanking Start Register (CR15), and the most and second-most significant bits are supplied by bit 5 of the Maximum Scan Line Register (CR09) and this bit of this register, respectively.</p> <p>This 10-bit value should be programmed to be equal to the number of scan lines from the beginning of the active display area to the beginning of the blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical blanking period begins.</p>
2	<p>Vertical Sync Start Bit 8. The vertical sync start is a 10-bit value that specifies the beginning of the vertical sync pulse relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Sync Start Register (CR10), and the most and second-most significant bits are supplied by bit 7 and this bit, respectively, of this register.</p> <p>This 10-bit value should be programmed to be equal to the number of scan lines from the beginning of the active display area to the start of the vertical sync pulse. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical sync pulse begins.</p>
1	<p>Vertical Display Enable End Bit 8. The vertical display enable end is a 10-bit value that specifies the number of the last scan line within the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Display Enable End Register (CR12), and the two most significant bits are supplied by bit 6 and this bit, respectively, of this register.</p> <p>This 10-bit or value should be programmed to be equal to the number of the last scan line within in the active display area. Since the active display area always starts on the 0th scan line, this number should be equal to the total number of scan lines within the active display area, minus 1.</p>
0	<p>Vertical Total Bit 8. The vertical total is a 10-bit value that specifies the total number of scan lines. This includes the scan lines both inside and outside of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Total Register (CR06), and the most and second-most significant bits are supplied by bit 5 and this bit, respectively, of this register.</p> <p>This 10-bit value should be programmed to be equal to the total number of scan lines, minus 2.</p>



1.6.10 CR08 - Preset Row Scan Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=08h)

Default:0UUU UUUUb (U=Undefined)

Attributes:Read/Write

7 6 54 0
Reserved (0)Byte PanningStarting Row Scan Count

Bit	Description																		
7	Reserved. Read as 0s.																		
6:5	<p>Byte Panning. This field holds a 2-bit value that selects number of bytes (up to 3) by which the image is shifted horizontally to the left on the screen. This function is available in both text and graphics modes.</p> <p>In text modes with a 9-pixel wide character box, the image can be shifted up to 27 pixels to the left, in increments of 9 pixels. In text modes with an 8-pixel wide character box, and in all standard VGA graphics modes, the image can be shifted up to 24 pixels to the left, in increments of 8 pixels. When the Nine dot disable bit of the VGA control register is set, the pixel shift will be equivalent to the 8-dot mode.</p> <p>The image can be shifted still further, in increments of individual pixels, through the use of bits [3:0] of the Horizontal Pixel Panning Register (AR13).</p> <table border="1"> <thead> <tr> <th colspan="3">Number of Pixels Shifted</th> </tr> <tr> <th>Bit [6:5]</th> <th>9-Pixel Text</th> <th>8-Pixel Text & Graphics</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0</td> <td>0</td> </tr> <tr> <td>01</td> <td>9</td> <td>8</td> </tr> <tr> <td>10</td> <td>18</td> <td>16</td> </tr> <tr> <td>11</td> <td>27</td> <td>24</td> </tr> </tbody> </table>	Number of Pixels Shifted			Bit [6:5]	9-Pixel Text	8-Pixel Text & Graphics	00	0	0	01	9	8	10	18	16	11	27	24
Number of Pixels Shifted																			
Bit [6:5]	9-Pixel Text	8-Pixel Text & Graphics																	
00	0	0																	
01	9	8																	
10	18	16																	
11	27	24																	
4:0	<p>Starting Row Scan Count. This field specifies which horizontal line of pixels within the character boxes of the characters used on the top-most row of text on the display will be used as the top-most scan line. The horizontal lines of pixels of a character box are numbered from top to bottom, with the top-most line of pixels being number 0. If a horizontal line of these character boxes other than the top-most line is specified, then the horizontal lines of the character box above the specified line of the character box will not be displayed as part of the top-most row of text characters on the display. Normally, the value specified by these 5 bits should be 0, so that all of the horizontal lines of pixels within these character boxes will be displayed in the top-most row of text, ensuring that the characters in the top-most row of text do not look as though they have been cut off at the top.</p>																		



1.6.11 CR09 - Maximum Scan Line Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=09h)

Default:00h

Attributes:Read/Write

7 6 5 4 0
 Double ScanningLine Cmp <9>Vert Blank Start <9>Starting Row Scan Count

Bit	Description
7	<p>Double Scanning Enable.</p> <p>0 = Disable. When disabled, the clock to the row scan counter is equal to the horizontal scan rate. This is the normal setting for many of the standard VGA modes.</p> <p>1 = Enable. When enabled, the clock to the row scan counter is divided by 2. This is normally used to allow CGA-compatible modes that have only 200 scan lines of active video data to be displayed as 400 scan lines (each scan line is displayed twice).</p>
6	<p>Line Compare Bit 9. This bit provides the most significant bit of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 4 of the Overflow Register (CR07) supplies the second most significant bit, and bits 7-0 of the Line Compare Register (CR18) supply the 8 least significant bits.</p> <p>Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part.</p> <p>When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display whatever data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display whatever data exists in the frame buffer starting at the first byte of the frame buffer.</p>
5	<p>Vertical Blanking Start Bit 9. The vertical blanking start is a 10-bit value that specifies the beginning of the vertical blanking period relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Blanking Start Register (CR15), and the most and second-most significant bits are supplied by this bit and bit 3 of the Overflow Register (CR07), respectively.</p> <p>This 10-bit value should be programmed to be equal to the number of scan line from the beginning of the active display area to the beginning of the blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical blanking period begins.</p>
4:0	<p>Starting Row Scan Count. This field provides all 5 bits of a 5-bit value that specifies the number of scan lines in a horizontal row of text. This value should be programmed to be equal to the number of scan lines in a horizontal row of text, minus 1.</p>



1.6.12 CR0A - Text Cursor Start Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Ah)

Default:00UU UUUUb (U=Undefined)

Attributes:Read/Write

7 6 5 4 0
Reserved (00)Text Cursor OffText Cursor Start

Bit	Description
7:6	Reserved. Read as 0.
5	Text Cursor Off. This cursor is the text cursor that is part of the VGA standard. This text cursor exists only in text modes, and thus, this register is entirely ignored in graphics modes. 0 = Enables the text cursor. 1 = Disables the text cursor.
4:0	Text Cursor Start. This field specifies which horizontal line of pixels in a character box is to be used to display the first horizontal line of the cursor in text mode. The horizontal lines of pixels in a character box are numbered from top to bottom, with the top-most line being number 0. The value specified by these 5 bits should be the number of the first horizontal line of pixels on which the cursor is to be shown.

1.6.13 CR0B - Text Cursor End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Bh)

Default:0UUU UUUUb (U=Undefined)

Attributes:Read/Write

7 6 54 0
Reserved (0)Text Cursor SkewText Cursor End

Bit	Description
7	Reserved. Read as 0.
6:5	Text Cursor Skew. This field specifies the degree to which the start and end of each horizontal line of pixels making up the cursor is delayed to compensate for internal pipeline delays. These 2 bits describe the delay in terms of a number character clocks. Bit [6:5] Amount of Delay 00 = No delay 01 = Delayed by 1 character clock 10 = Delayed by 2 character clocks 11 = Delayed by 3 character clocks



Bit	Description
4:0	Text Cursor End. This field specifies which horizontal line of pixels in a character box is to be used to display the last horizontal line of the cursor in text mode. The horizontal lines of pixels in a character box are numbered from top to bottom, with the top-most line being number 0. The value specified by these 5 bits should be the number of the last horizontal line of pixels on which the cursor is to be shown.

1.6.14 CR0C - Start Address High Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Ch)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Start Address Bits [15:8]. This register provides either bits 15 through 8 of a 16-bit value that specifies the memory address offset from the beginning of the frame buffer at which the data to be shown in the active display area begins. (default is 0) In standard VGA modes, the start address is specified with a 16-bit value. The eight bits of this register provide the eight most significant bits of this value, while the eight bits of the Start Address Low Register (CR0D) provide the eight least significant bits.

1.6.15 CR0D - Start Address Low Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Dh)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Start Address Bits [7:0] This register provides either bits 7 through 0 of a 16 bit value that specifies the memory address offset from the beginning of the frame buffer at which the data to be shown in the active display area begins. (default is 0) In standard VGA modes the start address is specified with a 16-bit value. The eight bits of the Start Address High Register (CR0C) provide the eight most significant bits of this value, while the eight bits of this register provide the eight least significant bits.

1.6.16 CR0E - Text Cursor Location High Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Eh)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Text Cursor Location Bits [15:8]. This field provides the 8 most significant bits of a 16-bit value that specifies the address offset from the beginning of the frame buffer at which the text cursor is located. Bit 7:0 of the Text Cursor Location Low Register (CR0F) provide the 8 least significant bits.



1.6.17 CR0F - Text Cursor Location Low Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=0Fh)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Text Cursor Location Bits [7:0]. This field provides the 8 least significant bits of a 16-bit value that specifies the address offset from the beginning of the frame buffer at which the text cursor is located. Bits 7:0 of the Text Cursor Location High Register (CR0E) provide the 8 most significant bits.

1.6.18 CR10 - Vertical Sync Start Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=10h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Vertical Sync Start Bits [7:0]. This register provides the 8 least significant bits of a 10-bit that specifies the beginning of the vertical sync pulse relative to the beginning of the active display area of a screen. In standard VGA modes, this value is described in 10 bits with bits [7,2] of the Overflow Register (CR07) supplying the 2 most significant bits. This 10-bit value should equal the vertical sync start in terms of the number of scan lines from the beginning of the active display area to the beginning of the vertical sync pulse. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical sync pulse begins.

1.6.19 CR11 - Vertical Sync End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=11h)

Default:0U00 UUUUb (U=Undefined)

Attributes:Read/Write

7 6 5 4 3 0

Protect Regs 0:7ReservedVert Int EnableVert Int ClearVertical Sync End

Bit	Description
7	Protect Registers [0:7]. Note that the ability to write to Bit 4 of the Overflow Register (CR07) is not affected by this bit (i.e., bit 4 of the Overflow Register is always writeable). 0 = Enable writes to registers CR[00:07]. (default) 1 = Disable writes to registers CR[00:07].
6	Reserved. In the VGA standard, this bit was used to switch between 3 and 5 frame buffer refresh cycles during the time required to draw each horizontal line.
5	Vertical Interrupt Enable. This bit is reserved for compatibility only. While this bit may be written or read, it's value will have no effect. Note that the VGA does not provide an interrupt signal which would be



Bit	Description
	connected to an input of the system's interrupt controller. Bit 7 of Input Status Register 0 (ST00) originally indicated the status of the vertical retrace interrupt. 0 = Enable the generation of an interrupt at the beginning of each vertical retrace period. 1 = Disable the generation of an interrupt at the beginning of each vertical retrace period.
4	Vertical Interrupt Clear. This is reserved for compatibility only. Note that the VGA does not provide an interrupt signal which would be connected to an input of the system's interrupt controller. 0 = Setting this bit to 0 clears a pending vertical retrace interrupt. This bit must be set back to 1 to enable the generation of another vertical retrace interrupt.
3:0	Vertical Sync End. This 4-bit field provides a 4-bit value that specifies the end of the vertical sync pulse relative to its beginning. This 4-bit value should be set to the least significant 4 bits of the result of adding the length of the vertical sync pulse in terms of the number of scan lines that occur within the length of the vertical sync pulse to the value that specifies the beginning of the vertical sync pulse (see the description of the Vertical Sync Start Register for more details).

1.6.20 CR12 - Vertical Display Enable End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=12h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Vertical Display Enable End Bits [7:0]. This register provides the 8 least significant bits of a 10-bit value that specifies the number of the last scan line within the active display area. In standard VGA modes, this value is described in 10 bits with bits [6,1] of the Overflow Register (CR07) supplying the two most significant bits. This 10-bit value should be programmed to be equal to the number of the last scan line within in the active display area. Since the active display area always starts on the 0th scan line, this number should be equal to the total number of scan lines within the active display area, minus 1.

1.6.21 CR13 - Offset Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=13h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Offset Bits [7:0]. This register provides either all 8 bits of an 8-bit value that specifies the number of words or DWords of frame buffer memory occupied by each horizontal row of characters. Whether this value is interpreted as the number of words or DWords is determined by the settings of the bits in the Clocking Mode Register (SR01). In standard VGA modes, the offset is described with an 8-bit value, all the bits of which are provided by this register. This 8-bit value should be programmed to be equal to either the number of words or DWords (depending on the setting of the bits in the Clocking Mode Register, SR01) of frame buffer memory that is occupied by each horizontal row of characters.



1.6.22 CR14 - Underline Location Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=14h)

Default:0UUU UUUUb (U=Undefined)

Attributes:Read/Write

7 6 5 4 0
 Reserved (0) Dword Count By 4 Underline Location
 Mode

Bit	Description															
7	Reserved. Read as 0.															
6	<p>DWord Mode.</p> <p>0 = Frame buffer addresses are interpreted by the frame buffer address decoder as being either byte addresses or word addresses, depending on the setting of bit 6 of the CRT Mode Control Register (CR17).</p> <p>1 = Frame buffer addresses are interpreted by the frame buffer address decoder as being DWord addresses, regardless of the setting of bit 6 of the CRT Mode Control Register (CR17).</p> <p>Note that this bit is used in conjunction with bits 6 and 5 of the CRT Mode Control Register (CR17) to select how frame buffer addresses from the CPU are interpreted by the frame buffer address decoder as shown below:</p> <table border="1"> <thead> <tr> <th>CR14[6]</th> <th>CR17[6]</th> <th>Addressing Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Byte Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>DWord Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>DWord Mode</td> </tr> </tbody> </table>	CR14[6]	CR17[6]	Addressing Mode	0	0	Word Mode	0	1	Byte Mode	1	0	DWord Mode	1	1	DWord Mode
CR14[6]	CR17[6]	Addressing Mode														
0	0	Word Mode														
0	1	Byte Mode														
1	0	DWord Mode														
1	1	DWord Mode														
5	<p>Count By 4.</p> <p>0 = The memory address counter is incremented either every character clock or every other character clock, depending upon the setting of bit 3 of the CRT Mode Control Register.</p> <p>1 = The memory address counter is incremented either every 4 character clocks or every 2 character clocks, depending upon the setting of bit 3 of the CRT Mode Control Register. . This is used in mode x13 to allow for using all four planes.</p> <p>Note that this bit is used in conjunction with bit 3 of the CRT Mode Control Register (CR17) to select the number of character clocks are required to cause the memory address counter to be incremented as shown, below:</p> <table border="1"> <thead> <tr> <th>CR14[5]</th> <th>CR17[3]</th> <th>Addressing Incrementing Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>every character clock</td> </tr> <tr> <td>0</td> <td>1</td> <td>every 2 character clocks</td> </tr> <tr> <td>1</td> <td>0</td> <td>every 4 character clocks</td> </tr> <tr> <td>1</td> <td>1</td> <td>every 2 character clocks</td> </tr> </tbody> </table>	CR14[5]	CR17[3]	Addressing Incrementing Interval	0	0	every character clock	0	1	every 2 character clocks	1	0	every 4 character clocks	1	1	every 2 character clocks
CR14[5]	CR17[3]	Addressing Incrementing Interval														
0	0	every character clock														
0	1	every 2 character clocks														
1	0	every 4 character clocks														
1	1	every 2 character clocks														
4:0	<p>Underline Location. This field specifies which horizontal line of pixels in a character box is to be used to display a character underline in text mode. The horizontal lines of pixels in a character box are numbered from top to bottom, with the top-most line being number 0. The value specified by these 5 bits should be the number of the horizontal line on which the character underline mark is to be shown.</p>															



1.6.23 CR15 - Vertical Blanking Start Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=15h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	Vertical Blanking Start Bits [7:0]. This register provides the 8 least significant bits of a 10-bit value that specifies the beginning of the vertical blanking period relative to the beginning of the active display area of the screen. In standard VGA modes, the vertical blanking start is specified with a 10-bit value. The most and second-most significant bits of this value are supplied by bit 5 of the Maximum Scan Line Register (CR09) and bit 3 of the Overflow Register (CR07), respectively. This 10-bit value should be programmed to be equal the number of scan lines from the beginning of the active display area to the beginning of the vertical blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which vertical blanking begins.

1.6.24 CR16 - Vertical Blanking End Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=16h)

Default:Undefined

Attributes:Read/Write

This register provides a 8-bit value that specifies the end of the vertical blanking period relative to its beginning.

Bit	Description
7:0	Vertical Blanking End Bits [7:0]. This 8-bit value should be set equal to the least significant 8 bits of the result of adding the length of the vertical blanking period in terms of the number of scan lines that occur within the length of the vertical blanking period to the value that specifies the beginning of the vertical blanking period (see the description of the Vertical Blanking Start Register for details).

1.6.25 CR17 - CRT Mode Control

I/O (and Memory Offset) Address:3B5h/3D5h (index=17h)

Default:0UUU0 UUUUb (U=Undefined)

Attributes:Read/Write

7	6	5	4	3	2	1	0
CRT Ctrl Reset	Word or Byte Mode	Address Wrap	Reserved (0)	Count By 2	Horizontal Retrace Select	Select Row Scan Cntr	Compat Mode Support

Bit	Description
7	CRT Controller Reset. This bit has no effect except in native VGA modes (non-centered). 0 = Forces horizontal and vertical sync signals to be inactive. No other registers or outputs are affected. 1 = Permits normal operation.
6	Word Mode or Byte Mode.



Bit	Description															
	<p>0 = The memory address counter's output bits are shifted by 1 bit position before being passed on to the frame buffer address decoder such that they are made into word-aligned addresses when bit 6 of the Underline Location Register (CR17) is set to 0.</p> <p>1 = The memory address counter's output bits remain unshifted before being passed on to the frame buffer address decoder such that they remain byte-aligned addresses when bit 6 of the Underline Location Register (CR17) is set to 0.</p> <p>Note that this bit is used in conjunction with bits 6 and 5 of the CRT Mode Control Register (CR17) to control how frame buffer addresses from the memory address counter are interpreted by the frame buffer address decoder as shown below:</p> <table border="1" data-bbox="261 573 1422 919"> <thead> <tr> <th>CR14[6]</th> <th>CR17[6]</th> <th>Address Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word Mode - Addresses from the memory address counter are shifted once to become word-aligned</td> </tr> <tr> <td>0</td> <td>1</td> <td>Byte Mode - Addresses from the memory address counter are not shifted</td> </tr> <tr> <td>1</td> <td>0</td> <td>DWord Mode - Addresses from the memory address counter are shifted twice to become DWord-aligned</td> </tr> <tr> <td>1</td> <td>1</td> <td>DWord Mode - Addresses from the memory address counter are shifted twice to become DWord-aligned</td> </tr> </tbody> </table>	CR14[6]	CR17[6]	Address Mode	0	0	Word Mode - Addresses from the memory address counter are shifted once to become word-aligned	0	1	Byte Mode - Addresses from the memory address counter are not shifted	1	0	DWord Mode - Addresses from the memory address counter are shifted twice to become DWord-aligned	1	1	DWord Mode - Addresses from the memory address counter are shifted twice to become DWord-aligned
CR14[6]	CR17[6]	Address Mode														
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1	1	DWord Mode - Addresses from the memory address counter are shifted twice to become DWord-aligned														
5	<p>Address Wrap. Note that this bit is only effective when word mode is made active by setting bit 6 in both the Underline Location Register and this register to 0.</p> <p>0 = Wrap frame buffer address at 16 KB. This is used in CGA-compatible modes.</p> <p>1 = No wrapping of frame buffer addresses.</p>															
4	<p>Reserved. Read as 0.</p>															
3	<p>Count By 2. This bit is used in conjunction with bit 5 of the Underline Location Register (CR14) to select the number of character clocks are required to cause the memory address counter to be incremented.</p> <p>0 = The memory address counter is incremented either every character clock or every 4 character clocks, depending upon the setting of bit 5 of the Underline Location Register.</p> <p>1 = The memory address counter is incremented either every other clock.</p> <table border="1" data-bbox="261 1381 1422 1644"> <thead> <tr> <th>CR14[5]</th> <th>CR17[3]</th> <th>Address Incrementing interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>every character clock</td> </tr> <tr> <td>0</td> <td>1</td> <td>every 2 character clocks</td> </tr> <tr> <td>1</td> <td>0</td> <td>every 4 character clocks</td> </tr> <tr> <td>1</td> <td>1</td> <td>every 2 character clocks</td> </tr> </tbody> </table>	CR14[5]	CR17[3]	Address Incrementing interval	0	0	every character clock	0	1	every 2 character clocks	1	0	every 4 character clocks	1	1	every 2 character clocks
CR14[5]	CR17[3]	Address Incrementing interval														
0	0	every character clock														
0	1	every 2 character clocks														
1	0	every 4 character clocks														
1	1	every 2 character clocks														
2	<p>Horizontal Retrace Select. This bit provides a way of effectively doubling the vertical resolution by allowing the vertical timing counter to be clocked by the horizontal retrace clock divided by 2 (usually, it would be undivided).</p> <p>0 = The vertical timing counter is clocked by the horizontal retrace clock.</p> <p>1 = The vertical timing counter is clocked by the horizontal retrace clock divided by 2.</p>															



Bit	Description
1	<p>Select Row Scan Counter.</p> <p>0 = A substitution takes place, where bit 14 of the 16-bit memory address generated of the memory address counter (after the stage at which these 16 bits may have already been shifted to accommodate word or DWord addressing) is replaced with bit 1 of the row scan counter at a stage just before this address is presented to the frame buffer address decoder.</p> <p>1 = No substitution takes place. See following tables.</p>
0	<p>Compatibility Mode Support.</p> <p>0 = A substitution takes place, where bit 13 of the 16-bit memory address generated of the memory address counter (after the stage at which these 16 bits may have already been shifted to accommodate word or DWord addressing) is replaced with bit 0 of the row scan counter at a stage just before this address is presented to the frame buffer address decoder.</p> <p>1 = No substitution takes place. See following tables.</p>

The following tables show the possible ways in which the address bits from the memory address counter can be shifted and/or reorganized before being presented to the frame buffer address decoder. First, the address bits generated by the memory address counter are reorganized, if need be, to accommodate byte, word or DWord modes. The resulting reorganized outputs (MAOut15-MAOut0) from the memory address counter may also be further manipulated with the substitution of bits from the row scan counter (RSOut1 and RSOut0) before finally being presented to the input bits of the frame buffer address decoder (FBIn15-FBIn0).

Memory Address Counter Address Bits [15:0]

	Byte Mode CR14 bit 6=0 CR17 bit 6=1 CR17 bit 5=X	Word Mode CR14 bit 6=0 CR17 bit 6=0 CR17 bit 5=1	Word Mode CR14 bit 6=0 CR17 bit 6=0 CR17 bit 5=0	DWord Mode CR14 bit 6=1 CR17 bit 6=X CR17 bit 5=X
MAOut0	0	15	13	12
MAOut1	1	0	0	13
MAOut2	2	1	1	0
MAOut3	3	2	2	1
MAOut4	4	3	3	2
MAOut5	5	4	4	3
MAOut6	6	5	5	4
MAOut7	7	6	6	5
MAOut8	8	7	7	6
MAOut9	9	8	8	7
MAOut10	10	9	9	8
MAOut11	11	10	10	9
MAOut12	12	11	11	10
MAOut13	13	12	12	11
MAOut14	14	13	13	12
MAOut15	15	14	14	13

X = Don't Care



Frame Buffer Address Decoder

	CR17 bit 1=1	CR17 bit 1=1	CR17 bit 1=0	CR17 bit 1=0
	CR17 bit 0=1	CR17 bit 0=0	CR17 bit 0=1	CR17 bit 0=0
FBIIn0	MAOut0	MAOut0	MAOut0	MAOut0
FBIIn1	MAOut1	MAOut1	MAOut1	MAOut1
FBIIn2	MAOut2	MAOut2	MAOut2	MAOut2
FBIIn3	MAOut3	MAOut3	MAOut3	MAOut3
FBIIn4	MAOut4	MAOut4	MAOut4	MAOut4
FBIIn5	MAOut5	MAOut5	MAOut5	MAOut5
FBIIn6	MAOut6	MAOut6	MAOut6	MAOut6
FBIIn7	MAOut7	MAOut7	MAOut7	MAOut7
FBIIn8	MAOut8	MAOut8	MAOut8	MAOut8
FBIIn9	MAOut9	MAOut9	MAOut9	MAOut9
FBIIn10	MAOut10	MAOut10	MAOut10	MAOut10
FBIIn11	MAOut11	MAOut11	MAOut11	MAOut11
FBIIn12	MAOut12	MAOut12	MAOut12	MAOut12
FBIIn13	MAOut13	MAOut13	RSOut0	RSOut0
FBIIn14	MAOut14	RSOut1	MAOut14	RSOut1
FBIIn15	MAOut15	MAOut15	MAOut15	MAOut15

1.6.26 CR18 - Line Compare Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=18h)

Default:Undefined

Attributes:Read/Write

Bit	Description
7:0	<p>Line Compare Bits [7:0]. This register provides the 8 least significant bits of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 6 of the Maximum Scan Line Register (CR09) supplies the most significant bit, and bit 4 of the Overflow Register (CR07) supplies the second most significant bit.</p> <p>Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part. (This register is only used in split screening modes, and this is not a problem because split screening is not actually used for extended modes. As a result, there is no benefit to extending the existing overflow bits for higher resolutions.)</p> <p>When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display whatever data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display whatever data exists in the frame buffer starting at the first byte of the frame buffer.</p>



1.6.27 CR22 - Memory Read Latch Data Register

I/O (and Memory Offset) Address:3B5h/3D5h (index=22h)

Default:00h

Attributes:Read Only

Bit	Description
7:0	Memory Read Latch Data. This field provides the value currently stored in 1 of the four memory read latches. Bits 1 and 0 of the Read Map Select Register (GR04) select which of the four memory read latches may be read via this register.



Revision History

Revision Number	Description	Revision Date
1.0	First 2012 OpenSource edition	May 2012

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