Intel Open Source Graphics Programmer's Reference Manual (PRM) for the 2013 Intel® Core™ Processor Family, including Intel HD Graphics, Intel Iris™ Graphics and Intel Iris Pro Graphics

Volume 4: Configurations (Haswell)

12/18/2013

Copyright

Configurations

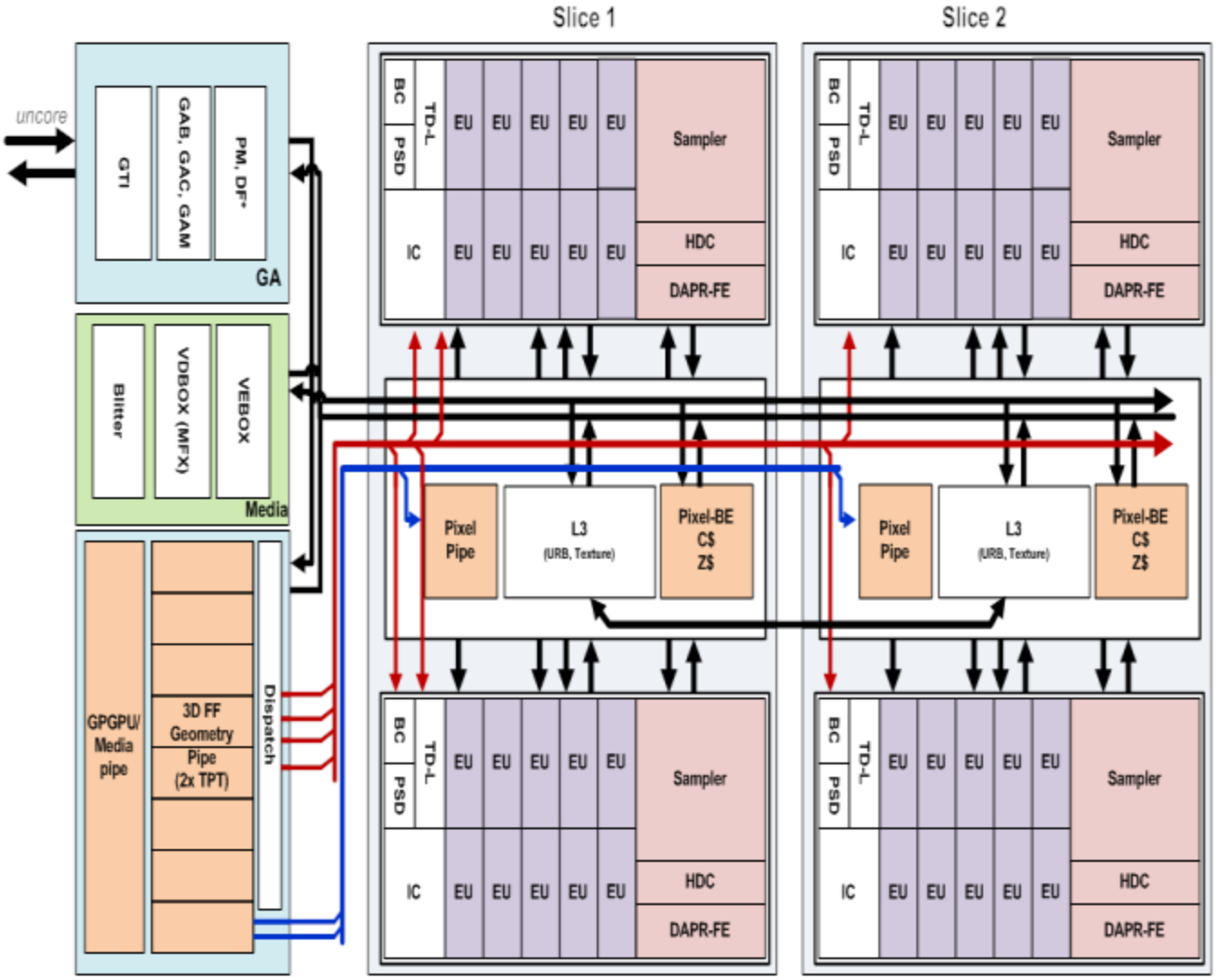
Table of Contents

Configurations Overview

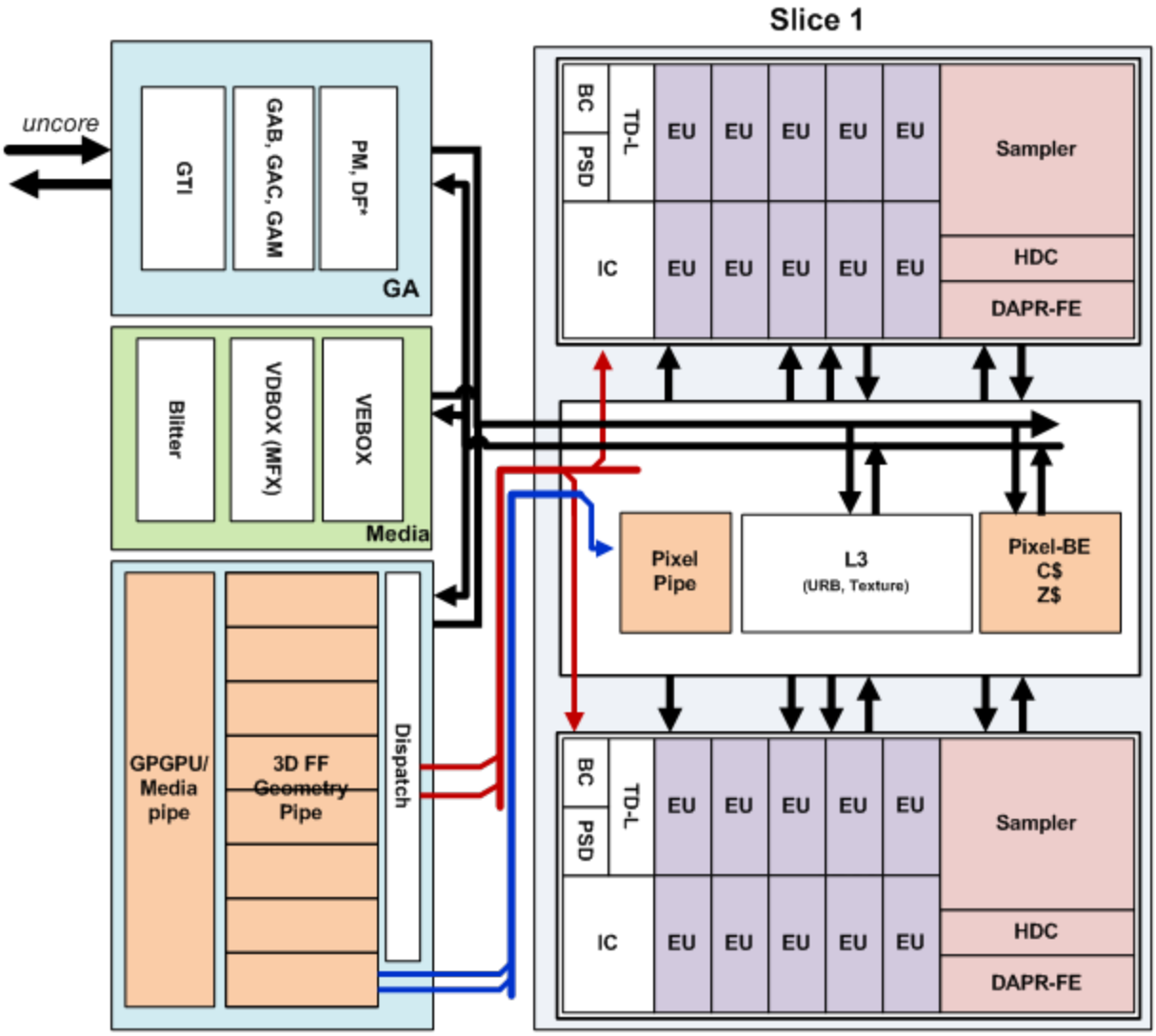
The Gen Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and its implementation have evolved to include many new features while achieving higher performance levels and increasing power efficiencies. This chapter tracks that evolution and provides generational information as to many basic architectural attributes. Further, for each generation, several variants of feature-set and/or performance may be released to the market, to which this chapter acts as a guide.

Top Level Block Diagrams

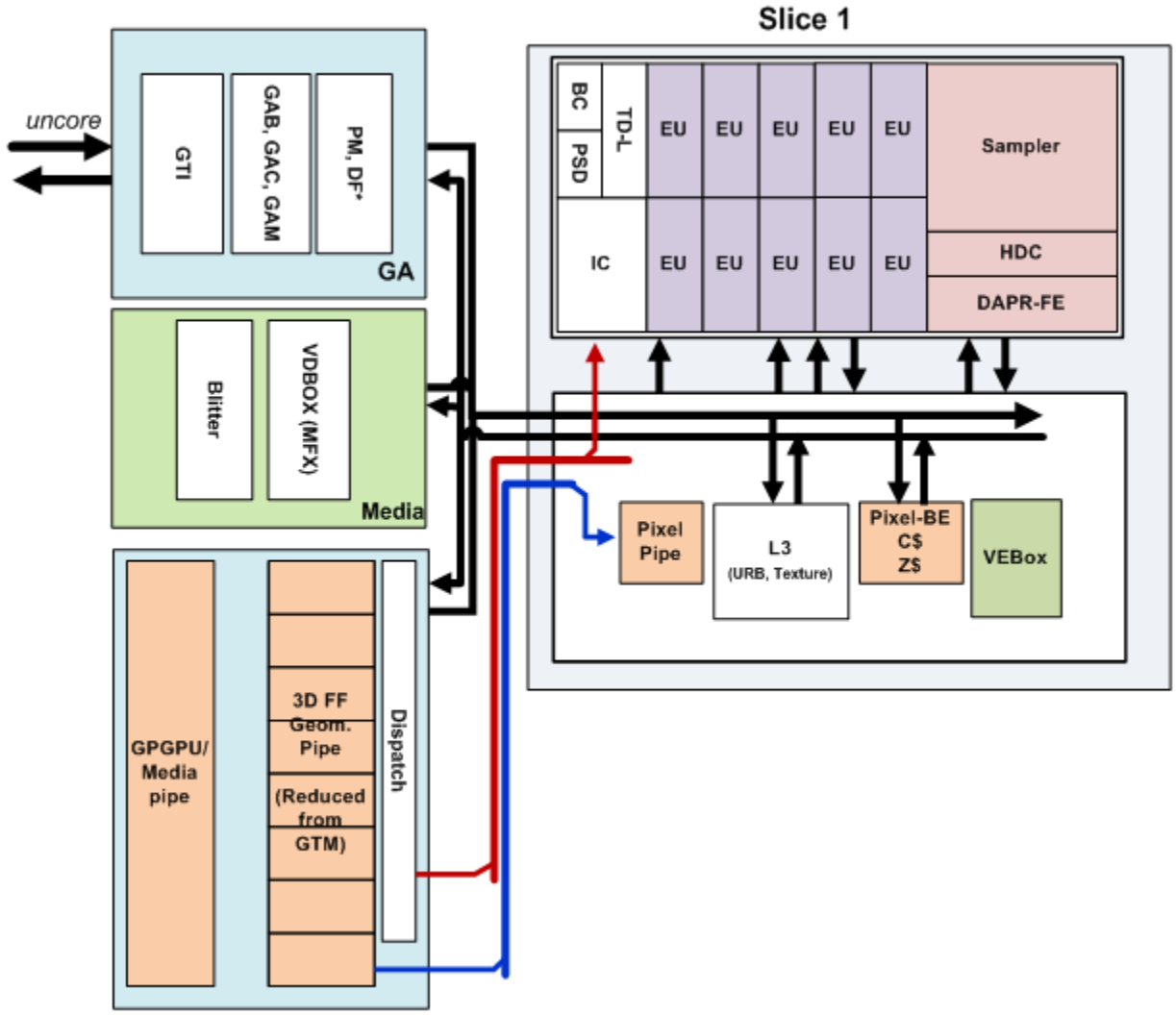
GT3 Top Level Block Diagram



GT2 Top Level Block Diagram



GT1 Top Level Block Diagram



Basic Configurations

With GT2 being a chop of GT3, any structure whose implementation exists across slices (e.g. L3$, URB) has its capacity reduced. Similarly any communication bus that services the second slice goes quiet. Such differences are called out in this table and other considerations are discussed further below.

Major Differences GT3, GT2, GT1

Description	GT3	GT2	GT1.5	GT1
Slice count	2	1	1	1
Subslice count	4	2	2	1
EUs (total)	40	20	12	10
Threads (total)	280	140	84	70
L3 Cache Size (total, URB + cache)	1024KB	512KB	512KB	256KB
URB Size (max, within L3$)	512KB	256KB	256KB	128KB
Cross-slice screen hash	16x16	None	None	None
Gateways	4	2	2	1
Thread groups outstanding (and associated SLM, barrier capacity)	64	32	32	
TDG Dispatch Bus	4	2	2	1
Push constants (capacity, granularity)	32K, 2K	16K, 1K	16K, 1K	16K, 1K
MSC layout for classic clear	Pixel grouping per slice	Everything contiguous	Everything contiguous	Everything contiguous
RCC behavior for R/W allocation	Partial for r/w cache lines	Full cache lines for r/w	Full cache lines for r/w	Full cache lines for r/w
SF Slice Filtering	Enabled	Disabled	Disabled	Disabled

Production HSW GT Versions

CPU Sku	Device 2 DID	RID
4+2 Standard (ext. PCH)	0x4XX	0x06
4+3e (Intel Iris™ Pro Graphics)	0xDXX	0x08
2+2 Standard (ext. PCH)	0x4XX	0x06
2+3 ULT	0xAXX	0x09
2+2 ULX (Standard Bin)	0xAXX	0x09
2+2 ULX (Lower Power Bin)	0xAXX	0x0B